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NASA-CR-54242
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SYSTEM CONTROL AND PROTECTION FOR PARALLELED STATIC CONVERTERS OR INVERTERS

CONTRACT NO. NAS 3-2792
AMENDMENT NO. 1

Fourth Quarterly Report For the Period
March 28, 1964 To June 27, 1964

PREPARED FOR THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

BY:
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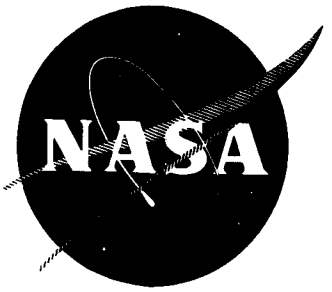

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Prepared for:

THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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ABSTRACT

This report describes the work completed during the fourth quarter of NASA Contract NAS3-2792, Amendment Number One. The following has been accomplished:

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A. The requirements for and limits of the automatic protection and paralleling of electrical systems whose power sources consist of static converters or inverters have been determined, and are included within the body of this report.

B. Truth tables and logic block diagrams showing the automatic protection and paralleling to be provided were prepared for both converter and inverter systems. These are shown in Charts I and II, and Figures III and V of this report.

C. Circuits have been designed to provide the automatic system protection and paralleling as required by the truth table and logic block diagrams referenced in paragraph B above. These circuits are shown in the schematic diagrams of figures IV and VI for static converter and inverter systems respectively.

D. Construction of breadboards, containing these automatic protection and paralleling circuits, to be used in system tests has been started. The following is required to complete the subject study and will be performed during the remaining portion of the subject contract.

1. Complete the construction of the breadboards containing the required protection and associated control circuits for paralleled converters or inverters. A total of four breadboards are to be built, two for use with paralleled converters and two for use with paralleled inverter systems.

2. Conduct laboratory tests on paralleled converter and paralleled inverter systems to demonstrate the capability of providing the required system protection as specified in Section III and IV of this report.

3. Complete the reliability analysis of both paralleled converter and paralleled inverter systems.

4. Provide a final report.

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SECTION I

INTRODUCTION

A. NASA Contract NAS 3-2792 was established to accomplish the following:

1. Improve inverter transformer weight and efficiency through the use of field-annealed doubly oriented silicon-steel magnetic core material (Cubex Steel).

2. Improve inverter-converter reliability and power capabilities by developing means for parallel operation of static inverters (DC-AC) and converters (DC-DC).

The results of this study are contained in three quarterly reports.[1, 2, 3*] As a part of item 2 above an analysis of the factors involved in achieving higher reliability and reduced weight in moderate power static inverter or converter systems was conducted. This analysis is contained in Section IV, pages 77 through 90 of the third quarterly report.[3] The analysis illustrated that any specified reliability could be precisely met if parallel operation was an established fact.

B. The capability to operate static inverters or converters in parallel was developed and demonstrated in the first portion of this contract. The results are contained in the third quarterly report.[3] However, operation of a parallel system requires that protection be provided to prevent loss of the entire system because of a fault occurring in the system. To provide this protection, Amendment No. 1 was added to the original contract.

The specific objectives of Amendment No. 1 are:

1. Determine and define the requirements necessary for reliable and efficient paralleling and protection of a power system consisting of two or more static converters or inverters.

2. Design the necessary circuits to provide the required paralleling and protection as determined and defined by 1. above.

*Refer to Bibliography within this report.

3. Demonstrate the capability of the designed circuits to protect and automatically parallel systems consisting of at least two static converters or inverters. Sufficient data shall be compiled to prove that reliable and efficient system protection and automatic paralleling have been accomplished.

In order to accomplish these objectives it was necessary to first establish basic ground rules of operation that the system must be capable of meeting. It was also necessary to define system limits for voltage, current and frequency that are to distinguish between normal and abnormal system operation. With the basic ground rules and system limits of operation established, a complete mode of system operation for both normal and abnormal conditions was established. These ground rules, system limits and system mode of operation are derived in Section II of this report.

From this mode of system operation a truth table was derived and used to minimize the circuit functions and prepare a logic block diagram to aid in the design of the required circuits. Separate truth tables and logic block diagrams were prepared for the converter and inverter systems. They are developed in Section III and IV respectively of this report.

Circuits to provide the required automatic paralleling and protection as defined by the truth tables and logic block diagrams were designed and are shown in the schematic diagrams of Figures IV and VI of this report for the converter and inverter systems respectively. These circuits are to be built and incorporated into breadboards to be used for system tests. A total of four breadboards are required. Two for use with the static inverter system and two with the static converter system. Construction of these breadboards has been started. The above work has been completed during the fourth quarter of this contract covering the period from 28 March 1964 to 27 June 1964. The results of this effort are contained within this report.

The breadboards are to be completed and used in performing system tests for both static inverter and static converter systems. The system tests are to demonstrate that automatic paralleling and protection have been provided in accordance with the requirements for system operation as established in this report. In addition to the system tests, a reliability analysis is to be made on the automatic paralleling and protection circuits utilized in the breadboards. The reliability analysis will consist of a stress analysis of critical parameters for critical components. Only steady state operating conditions at room ambient temperatures are to be considered.

Both the system tests and the reliability analysis are to be completed during the remainder of the program and the results provided in a final report.

SECTION II

SYSTEM PROTECTION

A. The main purpose of an electrical power system is to supply a load; however, many malfunctions or failures of individual system components as well as system faults may occur which will prevent the system from performing this purpose. It is impossible to provide a system that is required to perform over an extended period of time under severe operating conditions and be assured that nothing will occur during its operating life that will prevent the system from performing its basic function. Therefore, it is necessary that the system be designed to perform all or a major portion of its purpose with a given number of system failures occurring. Simply stated, the electrical power system must be reliable. The definition of reliability as it applies to a system is the probability that the system will perform its function within specified limits for a specified period of time under specified operating conditions. It is evident from the above definition that four conditions affect system design and must be defined.

First,the basic system functions must be defined. From this, basic ground rules can be established which will determine system operation. With system operation established, the necessary protection for the system can be determined. Second, the limits within which the system functions must be held by the protection determine the areas of normal and abnormal system operation and must be specified. Third, the operating time period of the system must be specified. Fourth, the conditions under which the system must operate, must be specified. The first and second items above dictate the basic system operation and design and apply in general to all types of system applications. Items three and four above are greatly determined by the individual application and affect the basic system philosophy only in the detailed design of individual system components. Therefore, in determining and defining the automatic paralleling and protection requirements for a system, only the first two items need be considered.

Any electrical power system may be considered to consist of two basic parts. One part is the power source with its associated control circuits that act to maintain the output power within specified limits. The second part is the load, which includes the distribution network through which the load is connected to the power source. Since both parts are susceptible to malfunction or failure, the effect on system operation for failures in either of these areas must be considered and a means to satisfy basic system requirements provided.

Since the power source is susceptible to failure, its failure would result in the loss of the entire electrical system if it consisted of only one power source. However, it was shown in the analysis of Section IV, pages 77 through 90, of the third quarterly report[3] that a system load can be supplied to any degree of reliability if parallel operation of static inverter or converter type power sources was an established fact. From this the following two ground rules are established.

1. The total power capacity of an electrical power system must consist of a number of power sources operating in parallel.

2. The entire system load must be capable of being supplied with the loss of a given number of power sources.

The results of the above referenced analysis can also be applied to the total system load. If the total system load were supplied from one common point, a failure at this point would appear as a total load fault and result in the loss of the entire system load. However, if the total system load was supplied as a number of smaller individual loads that could be isolated from the entire system in the event that a failure occurred on any of these individual loads, all the remaining loads could still be supplied power and function properly. From this the third basic ground rule for system operation is established and is as follows:

3. The total system load is to consist of a number of smaller individual loads.

In order to accomplish the above, selective isolation of system faults must be provided. This is accomplished by providing system protection that is capable of selective isolation of the faulted area while still maintaining maximum system load capability.

Prior to determining and defining the protection required, as well as the limits to be held, it is necessary to define protection. System protection is intended to prevent sustained abnormal or excessive transient conditions that may result in damage to or malfunction of either the systems utilization equipment or power sources. System protection is to be provided against abnormal system voltages, currents, and (for a-c systems only) frequencies. System protection will not adjust or regulate the basic system parameters to meet specified system limits, but will only sense the system parameters, determine if they are normal or abnormal, provide an allowable time for corrective action by the power source regulating circuits, and then, if the conditions are not corrected, act to isolate the fault while maintaining maximum system load capability.

The protection consists of two types. The first type provides protection for system failures that occur during system operation. An example of this type of protection is abnormal voltage protection. This protection will prevent abnormal voltage conditions from existing on the system. The second type of

protection provides protection by preventing operation of the system from occurring until certain conditions are satisfied. This prevents abnormal conditions from occurring. An example of this type of protection is the capability of automatically paralleling two power sources. This capability will prevent the paralleling of two power sources until specific conditions of their output power are satisfied. If the two sources were allowed to parallel without satisfying certain conditions, possible damage and/or failure of the entire system could result. From the above, the fourth basic ground rule for system operation is established.

4. System protection must be provided to isolate system faults before damage occurs to any other portion of the system while maintaining the capability to supply the maximum possible remaining system load.

From the above, the entire electrical power system is to consist of a number of sub-systems, each containing a power source, a portion of the total electrical load, and the required protection necessary to selectively isolate the faulted areas and maintain maximum system load capacity. Figures I and II are system schematics for paralleled converters and inverters respectively.

In any electrical power system the basic system parameters of voltage, current and frequencies (for a-c systems) are to be maintained within certain limits to assure compatibility between the systems power sources and utilization equipment. Any variation of the system parameters outside of these limits is considered an abnormal condition. A discussion of the causes of abnormal conditions and the action required to provide the necessary protection follows.

B. ABNORMAL VOLTAGE CONDITIONS.

System abnormal voltage conditions may occur for either isolated or paralleled system operation. For parallel system operation, abnormal voltage conditions result in an unbalance in load division between paralleled units. The results of this condition are basically an abnormal current condition and are discussed in Section II.C. of this report. For isolated system operation, abnormal voltage conditions may occur as either transient or continuous undervoltage or overvoltage conditions and abnormal voltage protection must be provided for the system.

Transient voltage conditions that exceed the nominal system voltage limits occur during normal system operation and are caused by the sudden applications or removals of large system loads or faults. The time duration is short and is an inherent characteristic of the transient response of the converter/inverter and its regulating circuit. During the original portion of this contract, system tests

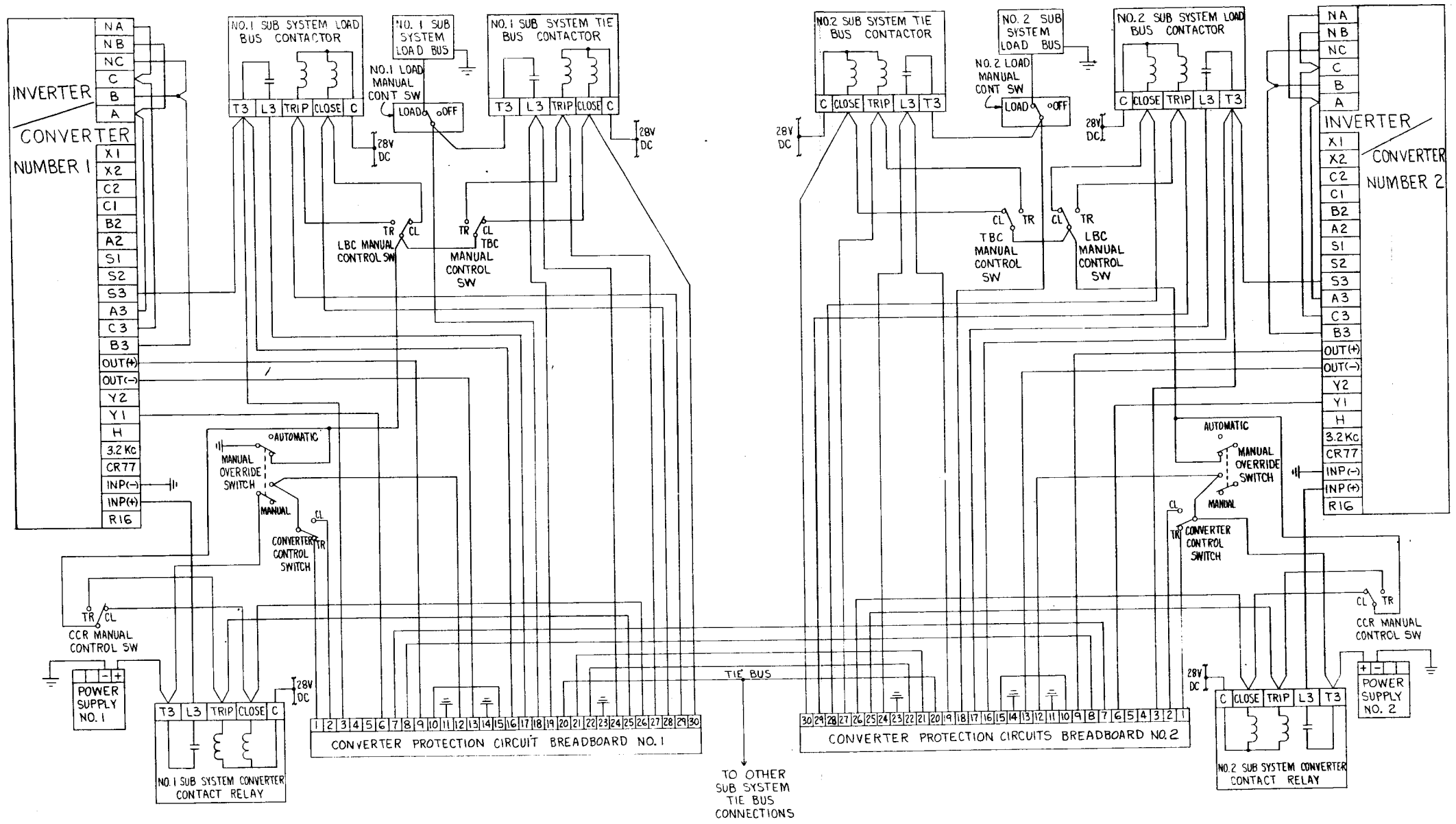

Figure I. Parallel Converter System Wiring Diagram

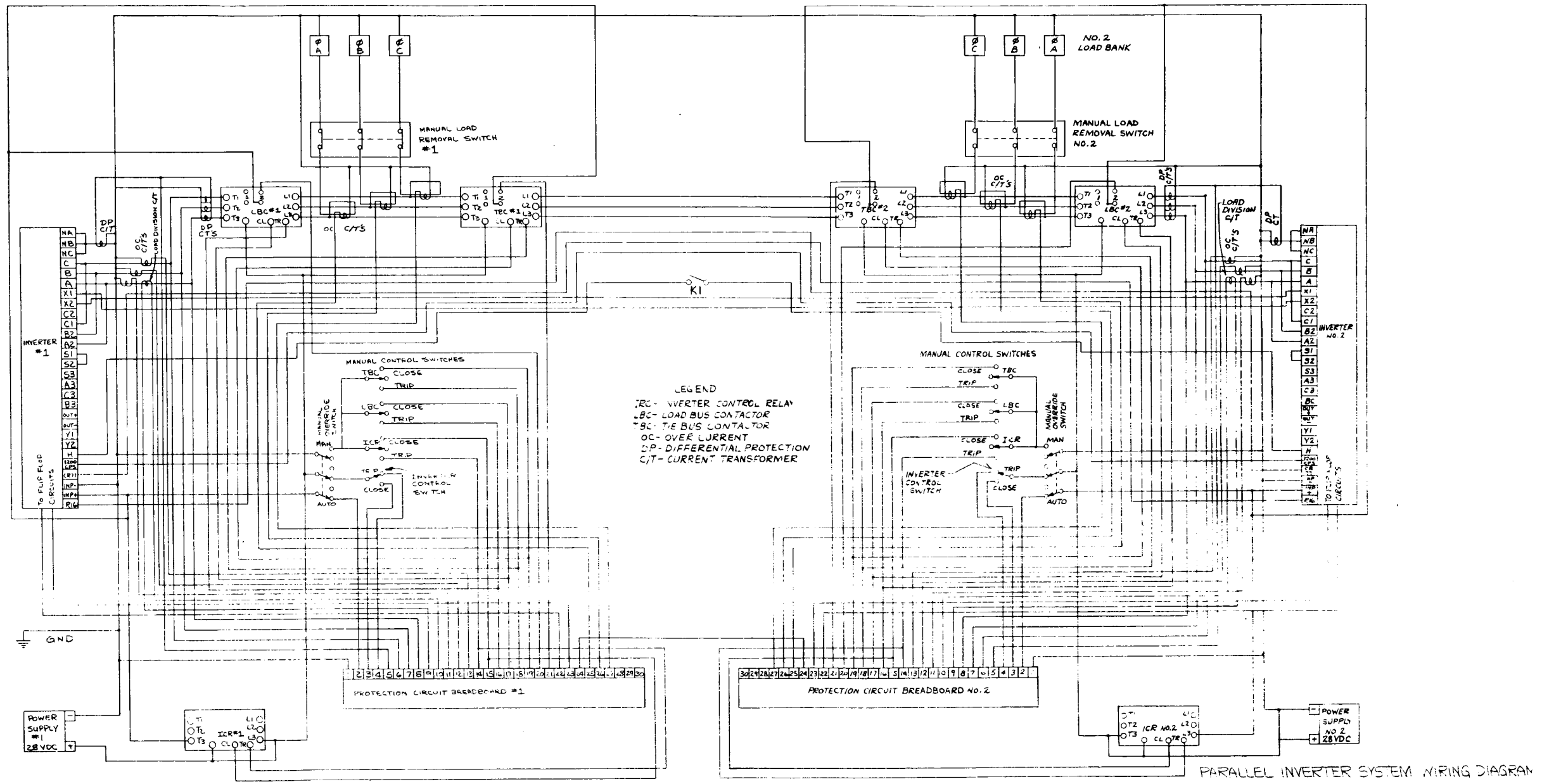

Figure II. Parallel Inverter System Wiring Diagram

were conducted where both static converters and inverters were paralleled under various conditions of initial system load. The results of these tests were recorded using oscillographs and show the transient response characteristics of the converters and inverters. The results of these tests are summarized in Appendix I of this report. From these results, the maximum time duration of the converter/inverter transient undervoltage or overvoltage conditions was determined to be 70 milliseconds. For undervoltage or overvoltage conditions that occur for this length of time, no damage will occur to the converter/inverter and the abnormal voltage protection must not operate. For conditions that result in the system voltage exceeding the nominal system voltage limits for periods greater than 70 milliseconds, a failure of the converter/inverter voltage regulating circuit is assumed. A failure of the voltage regulating circuit will provide a system voltage that may range anywhere from zero to a maximum voltage that is only limited by the power source and its regulating circuit. This condition is not tolerable and abnormal voltage protection must be provided to prevent damage or malfunction of the utilization equipment when it occurs. The maximum amount of time this condition may exist is determined by the utilization equipment. Since no voltage-time characteristics of utilization equipment has been specified, no specific maximum time can be stated. However, the main consideration is only that for abnormal voltage protection for utilization equipment this maximum time must be specified.

To provide the necessary system protection and prevent nuisance operations of the abnormal voltage protection, a means must be provided that will distinguish between the normal system transient conditions and the abnormal system voltage conditions. This is accomplished by a time delay. The length of this time delay must be compatible with the voltage-time characteristics of both the converter/inverter and that of the utilization equipment. It must be long enough to prevent nuisance operations of the abnormal voltage protection during normal transient conditions and short enough to prevent damage to the converter/inverter and utilization equipment. A maximum time for abnormal voltage of 250 milliseconds was selected in order to be compatible with feeder fault protection as described under abnormal current conditions of Section II.C. of this report.

Since an abnormal voltage condition that occurs during isolated system operation is a result of a failure in the voltage regulating portion of the converter/inverter, it is necessary that it be isolated from the sub-system load bus. However, to provide maximum system load capability it is required that the sub-system load be provided power to allow it to operate. This power is supplied to the sub-system load by connecting it to the system tie bus.

Summarizing, the abnormal voltage protection to be provided to the system is as follows. For system voltages that exceed the nominal system voltage by greater than 5% for a period of time greater than 250 milliseconds, the converter/inverter is to be de-energized and disconnected from the sub-system load bus. The sub-system load must then be connected to the system tie bus.

C. ABNORMAL CURRENT CONDITIONS.

Abnormal current conditions may occur during either parallel or isolated system operation. For parallel system operation, abnormal current conditions may be caused by a failure of the load division control circuit within the converter/inverter or by system feeder faults or system overloads. However, abnormal current conditions during isolated system operation can only occur because of a system fault. To provide reliable system operation that satisfies both the second and fourth basic system operating requirements, as given in Section II.A., of this report, adequate protection must be provided against these abnormal current conditions.

Prior to determining the protective action required for each of the above types of abnormal current conditions, their affect on system operation must be known. Each type is discussed below.

1. Parallel System Operation - Failure of the Load Division Control Circuit. For correct parallel system operation is is required that the system load be divided among converters/inverters in proportion to their respective load ratings. For units of equal load ratings the total system load should be divided as equally as possible. Failure to provide this capability may result in large load unbalances between converters/inverters and subsequent overload of the individual units. Since it is an inherent characteristic of static converters/inverters to share load in proportion to their internal voltage and impedance, and these may differ even between units of the same design and rating, large load unbalances between units may result. To prevent this from occurring, a means must be provided to adjust the internal voltages of the converters/inverters and force equal load division between paralleled units. During the first portion of this contract, circuits were designed to provide this load division control. An explanation of the operation of these circuits is contained in References 1, 2 and 3. Data showing the performance of these circuits during paralleled converter/inverter operation is also contained in Reference 3. From this data is was determined that the load division between two paralleled converters or inverters was able to be maintained at less than 10% of their nominal rated load, 0.22 amps for inverters and 0.5 amps for converters.

System protection is required to prevent large unbalances from occurring between paralleled units in the event that a failure of the load division control circuits occurs. Load unbalances between paralleled units may occur as either a transient or steady state condition. Load unbalances between paralleled units will occur for short periods of time without a failure of the load division control circuits. This happens when large system loads are applied or converters/inverters with various loads are paralleled. These unbalances occur because of the transient response characteristics of the load division control circuits and the

converters/inverters themselves. This is an inherent characteristic and load unbalances resulting from these conditions will not damage or affect the system operation or result in malfunction of the converters/inverters. The transient response characteristics of the load division control circuits were determined from the oscillograph recordings obtained during load division tests conducted on the first portion of this contract. The transient response characteristics are summarized in Appendix I of this report. The maximum duration of this transient response was 70 milliseconds.

In order to prevent nuisance operations of system protection, the load division protection circuits must be compatible with the transient response characteristics of the load division control circuits. This is accomplished by providing a fixed time delay that operates in conjunction with the load division protection circuits. This fixed time delay must be in excess of transient response characteristics of the load division control circuits but less than the maximum overload capability of the converters/inverters themselves. Since the maximum overload capability of the converters/inverters used for this program is 125% of rated (2.71 amps per phase for static inverters and 6.1 amps for static converters) for 5 minutes while providing rated output voltage, the time delay was arbitrarily set at 100 milliseconds to provide a realistic protection limit.

The load division protection circuit must also be compatible with the magnitude of overload capability of the converter/inverter. The overload capability was chosen as 120% of rated to provide a reasonable safety margin as explained under system overload capability in paragraphs 2 and 3, Section II.C. of this report. From the above, the load division protection to be provided will operate when the load unbalance between paralleled converters/inverters exceeds 10% to 20% of their rated load (between 0.22 and 0.42 amperes per phase for parallel inverters and between 0.49 and 0.98 amperes for parallel converters). Since the load unbalance is a result of a failure in the load division control circuit, the sub-system must be isolated from the remainder of the system. The system is then operated as an isolated system and will supply its own load.

In a converter system, the load division protection circuits must be sensitive to direct current unbalance only; however, in an a-c system, using inverters, the load division protection circuits must be sensitive to phase unbalance as well as absolute magnitude of current differences. Normally inverters are designed to share loads, within prescribed limits, over a predetermined load power factor range. If the load power factor is outside this range, the inverter load sharing circuits will not regulate properly. In this case the inverters may be operating at different phase angles. It is also possible for an inverter with faulted load sharing circuits to be supplying load at a different phase angle than the rest of the system because of faulted load sharing circuits. If this case exists, the inverter could be supplying or drawing large magnitudes of current to or from the

system without supplying its share of real power. Since any excessive currents can be damaging to the system, protection against excessive phase differences between inverters must be provided.

2. Parallel System Operation - System Faults. During parallel system operation feeder faults may occur anywhere within the system. A fault under this condition affects the entire system. If proper protection to isolate and remove the fault is not provided, loss of the entire system could result.

For faults that occur at different locations within the system, different fault protection is required. To aid in determining the fault protection required, the entire system is divided into three zones. The first zone includes the converter/inverter and all the distribution feeders up to the converter/inverter side of the load bus contactor. The second zone includes the sub-system load bus and all the distribution feeders between the load bus contactor and the tie bus contactor. The third zone, for each sub-system, includes the entire system on the tie bus side of the tie bus contactor.

The fault protection to be provided for each zone is intended to protect only the power sources and the distribution network and not the individual loads connected to each sub-system load bus. The protection for these individual loads must be provided by secondary protection which consists of circuit breakers, current limiters or fuses. The fault and overload characteristics of these devices closely match those of the individual load distribution feeders and provide selective fault isolation for individual load faults. A discussion of the fault protection and the action taken to isolate the fault for each of the three zones mentioned above is as follows:

a. ZONE ONE: The protection to be provided within this zone is intended to protect against feeder faults that occur on the output of the converter/inverter. This output extends to the load bus contactor by the distribution feeders since this is the first point at which the converter/inverter can be isolated from the system. The failures that occur within this zone are most likely very low impedance faults that will result in large fault currents. These fault currents could result in destroying the converter/inverter. No secondary protection is provided within this zone to clear the fault and there is no need to consider coordination between fault protection for this zone.

Static converter/inverter type power supplies have inherently low capabilities to support large overloads or fault currents, because of the low heat dissipation characteristics of the semiconductor devices that are used in their construction. Because of this

characteristic, these types of power sources usually contain a load limiting circuit to prevent the load current from exceeding a value that will either damage or reduce the useful life of the power source. The overload and short circuit capabilities of the converters/inverters used as part of this program cause the nominal output voltage to be maintained (115 volts line-to-neutral for inverters and 153.5 volts for converters) for load up to 125% of rated. The output voltage will then decrease to zero as the output load approaches 150% of rated. At this point the load limiting circuit limits the output load to 150% of rated and drives the output voltage to zero. The converter/inverter is capable of supplying 150% of rated load for five seconds. The current limiting circuit is sufficient protection to prevent damage to the power source for all types of faults that occur within zone one. However, in the event this circuit fails the maximum current capable of being supplied by the converters/inverters is limited only by their internal impedance and the fault impedance. This would provide a fault current large enough to destroy the converter/inverter. To prevent the above from occurring it is desirable to isolate the fault as quickly as possible. The protection required is to shut down the converter/inverter and open the load bus contactor. The tie bus contactor for the sub-system within which the fault occurred should remain closed in order to continue to supply the sub-system load.

b. ZONE TWO: During parallel system operation, faults that occur within this zone are supplied by both the sub-system converter/inverter and all other sub-systems connected to the systems tie bus. A fault within this zone could be a result of a fault on either the sub-system load bus that will be cleared by the secondary protection provided for individual loads or by a feeder fault that will not be cleared by the secondary protection. The system protection to be provided for this zone must distinguish between these two types of faults as well as coordinate with the secondary protection.

To provide coordination between system fault protection and individual load secondary protection a fixed time delay that operates in conjunction with system fault protection is provided.
The time delay must be long enough to allow the secondary protection to operate. If the fault is not removed within this time period the fault is assumed to be in the distribution feeder within this zone, and system protection must operate to isolate this zone from both the sub-system converter/inverter and the systems tie bus.

c. ZONE THREE: A fault occurring within this zone appears as a tie bus fault for each sub-system, while the fault may actually occur on either the tie bus or within zones one or two of any other sub-system. In any case, for any fault that occurs in which the sub-system supplies fault current through its tie bus contactor, the operation of system protection must coordinate with the other sub-systems and allow enough time for the other sub-systems to isolate and remove the fault. To provide this coordination, a fixed time delay that operates in conjunction with the system protection for this zone must be provided. The time duration must be long enough to allow the secondary protection for the individual loads on any sub-system to operate and clear the fault. This time delay was chosen as 150 milliseconds since it must also coordinate with abnormal voltage protection during isolated system operation.

For system faults that exceed 150 milliseconds, the fault is assumed to be on the tie bus and the sub-system must be isolated from the tie bus and operated as an isolated system.

3. Isolated System - Fault Protection. Protection against system faults must also be provided for isolated system operation. During isolated system operation, only zones one and two as defined in Section II.C. exist. The protection provided during parallel system operation is still operative and applicable to isolated system operation.

D. ABNORMAL FREQUENCY CONDITIONS. (For a-c systems only.)

Abnormal frequency conditions can occur anytime after start-up during both automatic isolated and parallel system operation. Abnormal frequency conditions during system parallel operation are the most dangerous since the out-of-phase condition between parallel inverters produced by this situation would cause dangerous current levels in the system and may result in complete system failure. In this respect, systems using inverters as power sources are different than those utilizing rotating generators. Once paralleled, a generator will, because of its inherent characteristics, remain locked in phase and in synchronism with the power system.

A frequency change in such a system is a continuous function and therefore, a frequency reference is not needed. However, in an inverter system, frequency changes can be abrupt. Also since the inverters will not lock on to the system output frequency as generators do, a system frequency reference and a means to lock on to this reference must be provided. Therefore, protection against failure of this reference must also be considered.

During start-up of an inverter, protection must be provided against the possibility that the frequency never becomes stable within specified limits. A possible cause of this type of failure would be a malfunction in the inverter frequency oscillator. Presence of this condition could render the inverter unusable in a parallel system, since it is doubtful that it could be reliably synchronized to a system frequency reference. Therefore, system protection must allow adequate time for the inverter frequency to become normal before action is taken to automatically shut it down. A time delay, described later in this report, is provided for this purpose. The over-under frequency circuit, described in Section IV is provided to lock out an inverter if its frequency is not normal at the end of the time delay or if it becomes out of limits during isolated operation.

A second type of frequency fault which may occur and can be detrimental to a parallel inverter system is failure of the frequency reference to which all paralleled inverters are synchronized. This type of failure would instantly allow all paralleled inverters to run at their own free-running oscillator frequency. This type of action would prevent the parallel system from acting as a usable power source since, at sometime, each inverter would because of its phase error be drawing power from the rest of the system instead of delivering power to it. Protection must be provided in case this fault occurs and it must result in immediate isolation of all sub-systems so that each inverter can supply its own load while operating on its own frequency oscillator. The frequency reference failure circuit, described in Section IV will provide protection against this fault.

System transients due to adding or removing sudden loads should not affect the frequency of an inverter especially if it is locked on to the system frequency reference; however, the circuits provided in this program will also provide system protection against this type of fault if it should occur.

The system tests conducted during the first portion of this contract did not cover the effects of unstable frequency conditions or system frequency reference failure. The above conclusions can be drawn, however, from what is known about systems in general and the particular circuits used in this system that would be involved in frequency fault conditions. It should be obvious, however, that system over-underfrequency limits cannot be generally established at this time.

One consideration here is the effects of system frequency instability upon frequency sensitive utilization equipment such as synchronous motors or gyro motors. Frequency changes in a system using inverters as power sources can be very abrupt. For example, failure of system main frequency reference to which all paralleled inverters are synchronized would result in the frequency of all inverters instantly being that of their own separate free running oscillators.

Since no frequency limits for utilization equipment have been specified an overfrequency trip point of 405 cps and an underfrequency trip point of 390 cps were arbitrarily chosen. The inverter unijunction oscillator frequency was chosen to be 395 cps nominally.

E. ASSOCIATED CONTROLS

In order to provide correct system operation as well as protection against the abnormal conditions as discussed in sections B, C and D above, certain associated controls are required. A brief description and discussion of each of these associated controls is provided below.

1. Converter/Inverter Control Contactor. A means must be provided to start-up and shut-down each sub-system converter/inverter. This is accomplished by connecting the converter/inverter to or isolating it from its power source. This control is provided by a latch-type contactor referred to as the converter/inverter control contactor. Whenever the converter/inverter is to be energized this contactor is closed and the converter/inverter is supplied power through a set of closed contacts. Whenever the converter/inverter is to be de-energized, the contactor is opened.

A brief description of the operation of a latch type contactor is provided in Appendix II.

2. Load Bus Contactor. A means must be provided to connect each sub-system converter/inverter to the sub-system load bus. This is accomplished by using another latch-type contactor which will be referred to as the load bus contactor. Whenever the load bus contactor is closed the converter/inverter will be connected to the sub-system load bus through a set of closed contacts. Whenever the load bus contactor is tripped these contacts will be opened isolating the converter/inverter from the load bus.

3. Tie Bus Contactor. The individual sub-systems will be interconnected to operate in parallel through a common tie bus. Each sub-system will be connected to the tie bus through a latch-type contactor referred to as the tie bus contactor. Whenever the tie bus contactor is closed, the sub-system will be connected to the tie bus through a set of closed contacts. Whenever the sub-system is to be isolated from the tie bus, this set of contacts is opened.

4. Power Ready. A power ready circuit will be provided to prevent connection of a converter/inverter to the sub-system load bus until its output power is within the limits of normal system operation as established in sections B, C and D above. No abnormal voltage, current or

(for inverter systems) frequency conditions must exist prior to connection of the converter/inverter to the load bus.

During system start-up a fixed time delay of 11 seconds is provided. This time delay is required in order to be compatible with the inherent start-up time of the static inverters used as part of this program. If a power ready condition is reached, anytime within this 11 second time delay, the converter/inverter is immediately connected to the sub-system load bus by closing the load bus contactor. If a power ready condition is not attained within this time limit, the converter/inverter will be de-energized by tripping the converter/inverter contactor and isolating from the sub-system load bus by preventing the load bus contactor from closing. The sub-system load will then be connected to the tie bus by closing the tie bus contactor.

5. Automatic Paralleling.

a. STATIC INVERTERS. Paralleled inverters in a system must meet the requirement, that each paralleled inverter must remain in phase with all other paralleled inverters at all times. Failure to meet this requirement will result in abnormal system currents which can cause the system to malfunction. If a single inverter is running at the system frequency but is paralleled out of phase with the system, it will be absorbing power from the system during the portion of its frequency cycle when its output voltage is low with respect to the rest of the system and will be delivering power to the system when its output voltage is higher. Not only is this situation bad from an efficiency standpoint but it can also cause at least one inverter to become damaged; therefore, a system which does not protect against such a condition will be extremely unreliable.

Another problem resulting from a phase difference between paralleled inverters is that frequency sensitive loads would have no reference upon which to synchronize, since they depend upon the rate of change of output voltage as a synchronizing reference. This reference would not be present in an abnormal output voltage wave shape produced by inverters paralleled out of phase; therefore, for successful operation it is mandatory that all inverters remain in phase with each other in a paralleled system.

Compliance with this requirement applies to all inverters; however, the methods used may differ for different types of inverters. The following discussion pertains primarily to the type of static inverters used in this program.

Automatic paralleling in an inverter system is done in a manner similar to that in a rotating generator system; however, paralleling inverters is more difficult and presents some unique problems.

The first problem with inverters, not generally found in rotating generation equipment, is the variation in the phase of inverter output voltage for changes in its load. Thus, an unloaded inverter being paralleled to a loaded system would almost immediately change phase at the time it is paralleled. This phase shift is because of the relatively large inverter output impedance as described in Appendix II of the third quarterly report.[3] Essentially, the inverter's sudden output current through its internal impedance causes this phase shift. Since inverters will not automatically bring themselves into synchronization with the system voltage when paralleled as generators do, successful paralleling must depend upon something other than the output voltage for a proper paralleling signal. The countdown circuits in a paralleled inverter maintain the same phase relative to the system regardless of the output phase shift due to load changes, thus, it is desirable to use a signal from these countdown circuits to parallel.

A second problem with inverters is the maximum phase angle between the countdown circuits of two inverters that will allow proper paralleling. It is necessary to make certain that an attempt to parallel an inverter to the system is done when its countdown circuits are almost exactly in phase with the countdown circuits of all paralleled inverters. A maximum difference of 1° is presently considered permissible with the inverters used in this program. This was determined by considering the type of paralleling signal produced by the inverters themselves. The signal is derived by passing the collector outputs of Q17A, Q17B, Q17C and Q17D and also the unijunction oscillator circuit output (Figure 4, page 9, 3rd Quarterly Report[3]) through an AND circuit to produce a 400 pulse per second paralleling signal. Since these pulses are about 15 microseconds wide, an overlap of at least 7 or 8 microseconds (about 1°) between the pulses of the inverter to be paralleled and the pulses of the already parallel inverters is deemed necessary for proper paralleling. This should allow the paralleling circuits of the oncoming inverter time to operate. Another reason for limiting the phase difference to a very few degrees when paralleling is that if paralleling is attempted at too large a phase difference the oncoming inverter will parallel 45 degrees or a multiple of 45 degrees out of phase with the rest of the system and remain there. This phenomenon is inherent in all of this type inverters and the reasons are discussed on page 8 of the third quarterly report[3].

The method to be used to parallel the inverters used in this program is briefly discussed below.

Each inverter has its own tuning fork frequency oscillator as a reference and its own separate unijunction oscillator. The tuning fork oscillator is much more stable than the unijunction oscillator; therefore, inverter frequency is usually derived by driving the unijunction oscillator with a tuning fork oscillator to maintain good frequency stability.

In the two inverter system, to be used for this program, one of the tuning fork oscillators will take precedence over the other by locking it out. As soon as the first inverter is started, its tuning fork frequency oscillator will start. The inverter will automatically be synchronized to it and placed on the line. When the second inverter is started it will operate from its unijunction oscillator until its countdown circuits become in phase with those of the first inverter. At this time it will also be locked in synchronism with the first tuning fork reference oscillator. The second inverter is then in phase with the first and will be automatically placed on the line. In a multi-inverter system, using this method, each succeeding inverter would be synchronized to the single tuning fork reference oscillator as described above.

If an inverter parallels out of phase with the rest of the system it will be automatically isolated and unlocked from the system frequency. It will then continue to supply its own load while operating on its unijunction oscillator. A more detailed description of this operation is given in Section IV of this report.

b. STATIC CONVERTERS. Automatic paralleling of two or more static converters is a less difficult task than automatic paralleling of static inverters. Only two conditions must be satisfied for paralleling of static converters. First, the output voltages of the power sources must be of the same polarity; and second, the magnitude of the output voltages must be nearly equal.

To assure proper polarity between converters the only requirement is that the correct mechanical connections be made when the converter is initially connected into the system. It is assumed that the converter will be given sufficient tests prior to installation in the system to determine that its output polarity is correct. The mechanical connections can be such that it is physically impossible to connect the converter into the system with incorrect polarity.

The second condition required for correct paralleling of static converters is to have the output voltages of the units to be paralleled as nearly equal as possible. The maximum voltage difference permitted between converters to be paralleled is determined by both the utilization equipment and the converter load division control circuit. For large voltage differences between converters, the load division unbalance will be large for a short period of time because of the transient response characteristics of the load division control circuit and the converters themselves. The smaller the voltage difference the smaller the load unbalance between units during the transient condition. The load division control circuit also has some maximum limit of control. Beyond this limit the control provided for load unbalances between paralleled units is no longer effective.

The transient condition created by paralleling converters with large differences in voltage is also affected by system load. The larger the load the greater the system disturbance. The system disturbance will show up as an undervoltage condition to the loads and an overload on the converter with the highest output voltage when it attempts to supply the entire load. The operation of utilization equipment is relatively unaffected if the transient condition is small and within given limits. However, if either of these limits are exceeded, the operation of the utilization equipment will be affected and it may malfunction.

Tests conducted during the first portion of this contract and the results contained in reference 3, indicate that the transient condition is affected more by system load than by voltage unbalance. The maximum voltage unbalance between units that were paralleled was 10 volts. The transient condition that resulted was very slight and did not appear to be near the limit of the load division control circuit. The limits for maximum voltage difference between converters to be paralleled will be set at the same value as the abnormal voltage limits of 146 to 161 volts. Since no limits are available for the maximum allowable transient conditions that utilization equipment can withstand this was not considered in the choice of the above limits.

F. SYSTEM OPERATION.

The description of system operation below pertains to both the inverter and converter systems.

1. Two methods of system operation are provided: (a) completely automatic, and (b) completely manual. Automatic system operation is the normal method of system operation. Manual system operation

is provided as a backup to automatic system operation and is intended to provide a means of system operation if the automatic operation and protection fail.

The method of system operation, automatic or manual, is selected by a switch referred to as the Manual Override switch provided for each sub-system. Whenever either method of operation for a sub-system is selected the other method is prevented from operating. The Manual Override switch is a three position switch. The three positions are Automatic, OFF, and Manual. When the switch is placed in the "Automatic" position, 28 volts d-c is supplied to the automatic protection and paralleling circuits and the Converter/Inverter Control switch. The sub-system is then ready for automatic operation. When the switch is placed in the "Manual" position, a ground circuit is provided through which the sub-system converter/inverter control relay, load bus contactor and tie bus contactor can be operated. In the "OFF" position, neither of the above conditions are provided and neither Automatic nor Manual operation is provided. A description of both methods of system operation is given below. The system schematic of Figures I and II is provided to illustrate system operation as detailed in the following descriptions.

2. Automatic System Operation. Automatic system operation provides start-up of the sub-system power source, connection of the power source to the load bus and paralleling of the sub-system with all the other sub-systems. During system operation it also provides automatically, all of the protection required for each sub-system.

Automatic system operation requires the use of only one switch in addition to the manual override switch. This is a three position switch and is referred to as the converter/inverter control switch. The purpose of this switch is to provide control in starting up or shutting down the sub-system. To start the sub-system, the converter/inverter control switch is placed in the "Close" position. This results in energizing the close coil of the converter/inverter relay and connecting input power to the converter/inverter through a set of contacts on the converter/inverter control relay. With input power applied to the converter/inverter the system is started. However, at this time no output is provided by the converter/inverter. Inherently, a given time is required for the converter/inverters themselves to build-up and provide an output. This time is required because of a time delay provided internal to the inverter/converter to allow the unit and its tuning fork reference to start and become stable. To be compatible with the inverter/converter, the automatic protection circuits must wait for this time delay. This is accomplished by providing a power ready circuit to prevent the sub-system from being connected to the load until a power ready condition exists. A power ready

condition is defined as a condition where no abnormal voltage, current or (for inverter systems) frequency exists.

If a power ready condition does not exist within eleven seconds after closing the converter/inverter control switch, a failure of the sub-system power source is indicated. The power source is then de-energized by operating the trip coil of the converter/inverter control relay. Since the failure is not a result of the sub-system load, the load must still be supplied power and allowed to operate. The load is connected to the system tie bus and supplied power from the remaining sub-systems through the tie bus. If a power ready condition is reached within eleven seconds, the power ready circuit is locked out and the sub-system power source is connected to the sub-system load bus. The power ready circuit also provides one other function during system start-up. As soon as power is provided to the automatic paralleling and protection circuits, the individual circuits will be ready to operate. Prior to a power ready condition, an undervoltage and underfrequency condition will exist (only undervoltage for converter systems). In order to prevent shutdown of the system because of this condition, the power ready circuit must prevent operation of the abnormal voltage or frequency protection until a power ready condition is reached. After a power ready condition is reached, the sub-system power source is connected to the sub-system load bus. The power ready lockout circuit is then disengaged and the abnormal voltage and frequency circuits are activated. The system is then operating as an isolated system. However, this system condition is only a temporary condition and the system immediately will attempt to obtain a parallel system connection. A parallel system condition is obtained by connecting the sub-system to the system tie bus. This is accomplished by either of two methods. If no other power source has been connected to the systems tie bus, the tie bus has no voltage. The first system is then connected to the tie bus through dead tie bus sensing circuits. This then provides a reference for all other sub-systems to compare their outputs with, to determine if conditions for paralleling power sources are satisfactory. This is accomplished by the automatic paralleling circuits. If the conditions for paralleling are satisfied, the sub-system is connected to the tie bus and parallel system operation is provided. For the inverter, where the conditions for voltage, frequency and zero phase angle between the oncoming sub-system and the system are satisfied, the power source is first locked to the system frequency and then connected to the tie bus for parallel system operation. When the system has reached a paralleled operating condition, the following protection is provided:

a. Load Division Protection
b. System Fault Protection

The system will continue to operate as a parallel system until some abnormal condition occurs. The appropriate system protection will then remove or isolate the abnormal condition and provide the system operation required.

Descriptions of the protection, control, and method of automatic paralleling provided are given in Sections III and IV following for the converter and inverter systems respectively.

3. Manual System Operation. Manual system operation is the secondary mode of operation and is provided to assure that the system can be operated in the event that automatic system operation is faulted. No protection is provided during manual system operation.

Manual operation is accomplished by placing the manual override switch in the manual position. This inactivates the converter/inverter control switch and permits the operation of three switches: the Inverter or Converter Control Relay switch (ICR or CCR), the Load Bus Contactor switch (LBC), and the Tie Bus Contactor switch (TBC). As their names imply, the ICR and the CCR control power to the inverter and converter, the LBC controls the power from the power source to the load, and the TBC controls connection of each sub-system to the tie bus.

For manual system operation, the inverter/converter is started by momentarily closing the ICR for inverters or the CCR for converters. The operator can monitor the inverter/converter output and determine when it shall be connected to the load by momentarily closing the LBC switch. The operator must also determine proper conditions for paralleling by monitoring inverter/converter outputs. He then must parallel the power sources by momentarily closing the TBC switch. Shutdown is accomplished by momentarily placing the TBC, LBC, and ICR/CCR switches in the trip position, in that order.

SECTION III

CONVERTER SYSTEM AUTOMATIC PROTECTION AND PARALLELING

Automatic protection for the abnormal system conditions described in Section II of this report as well as a description of the circuits used to provide automatic paralleling of static converters are contained within this section. The protection and automatic paralleling are provided by using only static circuits. No relays are used for any of the required sensing or logic circuits. Contactors are used for connecting the sub-system converters to their power supplies and load buses as well as connecting the sub-system to the system tie bus. These contactors are used because of the large amounts of power required to be controlled (approximately 750 VA per sub-system) and the unavailability of static type devices to replace contactors. A description of the individual circuits used to provide automatic protection and paralleling of static converters is provided below.

A. SYSTEM SWITCHES

Two switches are required for the operation of each sub-system within the entire electrical system. One switch is referred to as the Manual Override switch and provides a means to select one of the two methods of system operation. With the Manual Override switch placed in the "Automatic" position, d-c power is supplied to:

1. Activate the sub-system automatic protection and paralleling circuits.
2. Supply d-c power to the Converter Control switch.
3. Isolate the manual control circuits from ground, preventing their operation during automatic system operation.

To provide manual system operation, the Manual Override switch is placed in the "Manual" position. With the switch in this position, d-c power is removed from the automatic protection and paralleling circuits and the Converter Control switch, preventing their operation during manual system operation and providing a ground for the manual control circuits.

A second switch, referred to as the Converter Control switch, is also required for automatic system operation. This switch provides the means for start-up and shut-down of the sub-system.

Placing the converter control switch in the "CLOSE" position closes the converter control relay and connects the sub-system converter to its power supply. Start-up of the converter, connecting it to its load bus and automatically paralleling the sub-system with all other sub-systems is provided. All of the protection necessary for correct parallel or isolated system operation is then available.

The converter control switch also provides a means to shut the sub-system down. Placing the switch in the "TRIP" position will provide a signal to the automatic protection and paralleling circuits to:

1. Trip the sub-system converter control relay, de-energizing the converter.
2. Trip the sub-system load bus contactor, isolating the converter from the load bus.
3. Trip the sub-system tie bus contactor,isolating the sub-system from the system tie bus.

The operation of these two switches is illustrated in both Figures I and IV of this report.

B. CONVERTER CONTROL RELAY

Control of start-up or shut-down of a sub-system converter is provided by a two-coil, latch-type relay. When the close coil of the relay is operated, power is connected to the converter through a set of closed contacts on the converter control relay. This coil is operated whenever the converter control switch is placed in the close position. A lockout of this close signal is provided by the automatic protection and paralleling circuits to prevent cycling of the sub-system converter. Without lockout of the close signal, the converter of a sub-system might cycle if the converter control switch were held in the close position and a system fault occurred that provided a signal to shut-down the sub-system converter. The sub-system would be shut down, the system fault removed and a signal to close the converter control relay again applied. When the converter was again started, and if the system fault remained, the above would again occur. This would be repeated as long as the converter control switch was held in the close position with the system fault remaining. To prevent this, a lockout of the close signal to the converter control relay is provided by the automatic protection and paralleling circuits for any abnormal system condition that requires tripping of the converter control relay. This lockout signal is only removed when the Manual Override switch is placed in the "OFF" position, thereby removing d-c power to the automatic protection and paralleling circuits.

Operation of the circuits which provide control for the converter control relay is shown in the block marked "CCR Control" of Figure IV of this report.

C. POWER READY

System protection is provided to prevent connection of a converter to a load until the output of the converter is within the nominal system voltage limits of 146 to 161 volts. This protection is provided by a power ready circuit.

When the sub-system is started by placing the converter control switch in the "CLOSE" position, a signal is provided to the power ready circuit starting a fixed time delay. This time delay is referred to as TD2 and has a magnitude of 11 seconds. The purpose of this time delay is to enable the converters to start and provide an output. The converters utilized as a part of this program have an inherent time delay of approximately 10 seconds to allow stabilization of their tuning fork reference prior to providing an output.

If the converter output voltage comes within nominal system limits, prior to the duration of TD2, the power ready circuit provides output signals to:

1. Close the sub-system LBC, connecting the converter to the load bus.
2. Provide a lockout to the power ready circuit, preventing any output signals which would have occurred if a power ready condition had not been reached within the time duration of TD2.

If the converter output voltage does not reach a power ready condition prior to completion of TD2, a failure of the converter is assumed and the time delay circuit provides output signals to:

1. Trip the sub-system CCR, de-energizing the converter.
2. Lockout any signal to close the sub-system CCR.
3. Lockout any signal to close the sub-system LBC, assuring isolation of the converter from the sub-system load bus.
4. Close the sub-system TBC, connecting the sub-system load to the system tie bus.

The circuits utilized to provide power ready protection are shown in Figure IV on the portion of the circuit marked "Power Ready Protection".

D. LOAD BUS CONTACTOR CONTROL

Control for the connection to or isolation of the sub-system converter from its load bus is provided by a load bus contactor. The load bus contactor is a latch type contactor identical to the converter control relay. Control of both the

contactor close and trip coils is provided by the automatic protection or paralleling circuits. Whenever the close coil of the contactor is operated, the converter is connected to its load bus through a set of closed contacts. The close coil is operated by the Power Ready Protection Circuit, whenever the output power of the converter is within the voltage limits of 146 to 161 volts. The operation of the load bus contactor trip coil results in isolating the sub-system converter from the sub-system load bus. The trip coil is operated whenever an abnormal voltage condition exists during isolated system operation, a feeder fault occurs in zones one or two, or when a trip signal is received for system shut-down by the converter control switch. A lockout is provided for the close signal to the load bus contactor to prevent cycling during system operation. The lockout operation is similar to that described for the converter control relay in Section III. B. of this report.

Operation of the circuits which provide the above control for the load bus contactor are shown in the block marked "LBC Control" of Figure IV of this report.

E. ABNORMAL VOLTAGE PROTECTION

System protection against abnormal voltage conditions is provided for isolated system operation only. During parallel system operation, abnormal voltage conditions result in load unbalances between parallel units and system protection is provided by the load division protection circuit.

System protection against abnormal voltages is provided by a voltage sensing circuit which senses the sub-system voltage at the point of regulation (Figure I). The voltage is compared to two Zener reference diodes. One Zener reference diode is used to detect an undervoltage condition; the other an overvoltage condition. When either an undervoltage condition (system voltage less than 146 volts) or an overvoltage condition (system voltage greater than 161 volts) exists, a signal is provided from the voltage comparator circuits starting a fixed time delay referred to as TD1. This fixed time delay has a duration of 250 milliseconds. If the abnormal voltage condition exists for a period of time longer than 250 milliseconds, failure of the converter voltage regulating circuit is assumed. To remove the abnormal voltage condition and still supply power to the sub-system load, signals are provided by the time delay circuit to:

1. Trip the converter control relay (CCR), de-energizing the sub-system converter.
2. Lockout any signal to close the CCR.
3. Trip the sub-system load bus contactor (LBC), isolating the sub-system from its load bus.

4. Lockout any close signal to the LBC.
5. Close the sub-system tie bus contactor.

The circuit used to provide abnormal voltage protection is shown in Figure IV in the portion of the circuit marked "Abnormal Voltage".

F. TIE BUS CONTACTOR

The control for a sub-system which connects it to or isolates if from the system tie bus is provided by the tie bus contactor. This is a two-coil, latch-type contactor identical to the converter control relay and load bus contactor. Whenever the close coil is operated, the sub-system is connected to the tie bus through a set of closed contacts on the tie bus contactor. The operation of the close coil is controlled by the automatic protection and paralleling circuits provided for each sub-system. The close coil is operated by the automatic paralleling circuit when the conditions for either dead tie bus protection or automatic paralleling are satisfied. These conditions are described later in this report (paragraph G. of this section).

The trip coil is operated by the load division protection circuit, by automatic protection against faults occurring in zone 3, or when a trip signal is supplied by the sub-system converter control switch to shut the sub-system down. A lockout circuit is provided for the contactor close signal to prevent cycling during system operation when an abnormal condition or system fault occurs. The lockout circuit operates similarly to the lockout circuit described for the converter control relay.

The circuits used to provide the above control of the tie bus contactor are shown in Figure IV in the block marked "TBC Control".

G. AUTOMATIC PARALLELING OF STATIC CONVERTERS.

To correctly parallel two or more static converters two basic requirements must be satisfied. First, the polarity of the two sources must be the same. Second, the voltage magnitudes of the two sources must not differ by more than an amount beyond which the converter load division control circuits are no longer effective. The voltage difference also must be small to minimize the system disturbances caused by the transient response characteristics of the converters and their load division control circuits.

The condition of correct polarity can be satisfied by sufficient testing of the converter prior to installation in the electrical system and by restrictions on the mechanical connections required for actual installation of the converters

within the system. The remaining requirement of limiting the differences in voltage magnitude between the two converters to be paralleled must be satisfied electrically.

The method used to operate converters in parallel is to connect all the converters to a common bus. This bus is referred to as the system tie bus (Figure I). During initial system start-up, the converter which is started first is connected to its load bus when a power ready condition is reached. At this time the system tie bus voltage is sensed by the dead bus sensing portion of the automatic paralleling circuit to determine if any other sub-system is connected to the tie bus or if any voltage exists on the tie bus. If the tie bus voltage does not exceed 5 volts it is assumed that no other sub-system is connected to the tie bus and one sub-system may be connected to the tie bus. When this condition is satisfied the dead tie bus protection circuit provides a signal to:

1. Close the sub-system TBC, connecting the sub-system to the tie bus.
2. Close the load division control circuit.
3. Actuate the sub-system load division protection circuit.

The circuits used to provide this tie bus protection are shown in Figure IV in the block marked 'DTB". After one sub-system is connected to the tie bus, a reference is provided for all other sub-systems to which they compare their output and determine if the two converters should be paralleled. The next sub-system when, started and connected to its load bus, senses both its voltage at the point of regulation and the system tie bus voltage. Two different voltage sensing circuits are used that are identical to the abnormal voltage sensing circuit previously described. The voltages at these two points are then each compared to Zener reference diodes. If the voltage at either of these two points is outside of the power ready voltage limits (146 to 161 volts) the maximum voltage difference of 15 volts is exceeded and the conditions for paralleling are not satisfied. If the voltage at both of these two points is within the power ready voltage limits, the two power converters may be paralleled. When this condition exists, a signal is provided by the automatic paralleling circuit to:

1. Close the TBC of the sub-system that is not connected to the tie bus, paralleling the two sources.
2. Close the load division control circuit for the system that is to be connected to the tie bus.
3. Lockout the abnormal voltage protection circuit.
4. Actuate the load division protection circuit
5. Actuate the load division control circuit.

The two sub-systems will now operate in parallel until an abnormal system condition occurs which results in isolating the sub-systems.

The circuits to provide automatic paralleling are shown in Figure IV in the blocks marked "Load Bus Voltage AP, Tie Bus Voltage AP, AP-DTB Logic, Load Division Protection and Load Division Control".

H. LOAD DIVISION PROTECTION.

For correct operation of paralleled converters the system load must be divided nearly equal between the units. Inherently, static converters will share load in proportion to their internal voltage and impedance. Since these may differ even between units of the same rating and design, large unbalances in load may occur between units. To force equal division of the systems between paralleled converters, load division control circuits are provided within each converter which adjust their internal voltages and compensate for the differences in their internal impedances. If these circuits should fail, large unbalances in load division between units would result. System protection must be provided to prevent these large unbalances in load division in the event the load division control circuit should fail.

A load division protection circuit that senses the difference in load current between paralleled converters is used to provide the required protection. The converter output load current of each sub-system is sensed using a transductor circuit. The transductor circuit provides an output voltage that is proportional to the converter outputs load. The output of the transductor circuits for each converter operating in parallel are then connected in parallel in order to compare their output voltages. When the output current of each converter is equal the output voltage of each transductor circuit is equal and no current will flow between the paralleled branches of the load division protection loop. When the output current of one or more converters is less than or more than the other converters a voltage difference exists between the parallel branches of the load division protection loop, causing a current to flow in each of the paralleled branches of the loop. This branch current is proportional to the difference in load current of the converters. The magnitude of the branch current is then sensed for each converter. When it exceeds a value equivalent to a load current difference between paralleled converters of 0.5 to 1.0 ampere an output signal is provided to:

1. Trip the sub-system TBC, isolating the sub-system from the tie bus.
2. Lockout any close signal to the sub-system TBC.
3. Isolate the sub-system load division control circuit from the other sub-system load division control circuits.
4. Isolate the sub-system load division protection circuit from the other sub-system load division protection circuits.
5. Remove the parallel system operation lockout of the sub-system abnormal voltage protection.

These actions isolate only the sub-system that was supplying more or less than 0.5 to 1.0 amperes of the total system load than the other paralleled converters. The sub-system will continue to operate as an isolated system supplying its own load.

The circuits used to provide the above protection are shown in Figure I V in the blocks marked "Load Division Protection, Load Division Control, Transductor Elements identified as T7 and T9, and Transformer T8". Figure X I I of Appendix I V shows the required interconnections for the converter system load division protection circuits.

I. ABNORMAL CURRENT PROTECTION.

System protection against abnormal current conditions must be provided for both parallel and isolated system operating conditions. Abnormal current conditions may result during parallel system operation because of either a system fault or a failure in the converter load division control circuit. The protection provided must be capable of distinguishing between the two types of failures. Protection against system faults is described in this section and abnormal current conditions caused by the failure of the load division control circuit were discussed in Section H.

Abnormal current conditions occurring during isolated system operation are the result of system faults. The protection provided for system faults occurring during isolated system operation are also discussed below.

1. System Protection for Feeder Faults Occurring Within Zone One. (Reference Section II. C. 1.). To provide protection for faults occurring within this zone, current is sensed at two different points within the zone. One point is located in the ground return lead of the converter and the other at the load bus contactor on the converter side. During normal system operation the current through these two points is the same. When a difference in current exists, a fault exists within this zone. Protection is provided for Zone One by sensing the difference current.

To sense the current at these two points, a transductor circuit is used which has an output voltage proportional to the converter output current. The output voltages of the two transductor devices used are matched by adjustment so that for equal currents their output voltages are equal. For differences in currents, their output voltages will differ. To sense this difference, a differential amplifier is used. The characteristics of a differential amplifier are such that it compares two input voltages and provides an output signal proportional in magnitude to the difference between the two input voltages. When the difference between the two load currents exceeds 0. 5 ampere, the differential amplifier provides an output signal to:

a. Trip the sub-system CCR, de-energizing the converter.
b. Lockout any close signal to the CCR.
c. Trip the sub-system LBC, isolating the fault from the remaining portion of the system.
d. Lockout any close signal to the LBC.

For maximum system protection as well as efficiency and reliability, it is desirable to remove a fault within this zone as quickly as possible. Since no secondary protection is provided within this zone to remove the fault condition, no coordination of protection is required; therefore, no time delay, other than that inherent within the differential current sensing circuit, is provided.

The protection provided for faults occurring within Zone One for parallel system operation is identical to that required for isolated system operation. No additional or different protection is required.

The circuits used to provide the above protection are shown in Figure IV in the blocks marked CS1, CS2, Differential Current Protection and DCP - LB OC TD4. The Master Royer Oscillator circuit and transductors T3 and T4 also shown in Figure IV.

2. System Protection for Feeder Faults that Occur Within Zone Two. (Reference Section II.C.1.). System faults occurring within Zone Two of the system may be caused by either an individual load on the sub-system load bus, which should be cleared by the secondary protection, or by a fault within this zone where no secondary protection is provided. During parallel system operation, a fault within this zone will be supplied by both the sub-system converter and the system tie bus. This zone must then be completely isolated from the entire system.

Overcurrent sensing is utilized to provide protection and isolate the system fault. Both the current supplied from the sub-system converter and the current supplied from the system tie bus are sensed by transductor circuits identical to those utilized for differential current sensing in Zone One.

The output voltages of each transductor circuit are compared to a Zener diode reference. When the current sensed by both transductor circuits exceeds the overcurrent rating of the converter, which is 120% of rated (5.9 amperes), an output signal is provided to:

a. Lockout the operation of the load bus overcurrent protection.
b. Start a fixed time delay of 150 milliseconds. This time delay is referred to as TD5.

If the fault condition is not cleared within 150 milliseconds, a signal is provided by TD5 to:

a. Trip the sub-system TBC, isolating the sub-system from the tie bus.
b. Lockout any close signal to the TBC.

c. Lockout any close signal to the load division control circuit.
d. Remove the parallel system operation lockout for abnormal voltage protection.

The system tie bus then stops supplying the fault within zone two; however, the sub-system converter continues to supply this fault. The load bus overcurrent circuit is no longer locked out by the tie bus overcurrent sensing circuit, since it no longer sees the fault, and provides a signal to start a fixed time delay of 150 milliseconds. This time delay is referred to as TD4. If the fault condition is not removed within this time period, a signal is provided by the time delay to:

a. Trip the CCR, de-energizing the sub-system converter.
b. Lockout any close signal to the CCR.
c. Trip the LBC, isolating the sub-system converter from the load bus.
d. Lockout any close signal to the LBC.

When the above is completed, Zone Two is entirely isolated from the sub-system converter and the system tie bus.

During isolated system operation the sub-system would be isolated from the system tie bus. A fault occurring within Zone Two would cause only the load bus overcurrent sensing circuit to sense the overcurrent condition and provide a signal to:

a. Start time delay TD4.

If the fault is not cleared within the time duration of TD4, the time delay will provide a signal to:

b. Trip the CCR, de-energizing the sub-system converter.
c. Lockout any close signal to the CCR.
d. Trip the LBC, isolating the converter load bus.
e. Lockout any close signal to the LBC.

For a fault occurring within zone two during isolated system operation the converter output voltage will drop below 146 volts for fault currents that exceed 6.1 amperes (125% of rated). This undervoltage condition condition will be sensed by the abnormal voltage protection circuit which is not locked out during isolated system operation, and may operate. Since the operation of the abnormal voltage circuit transfers the sub-system load to the system tie bus, its operation during a zone two fault would simply transfer the fault to the system tie bus. This is undesirable and must be prevented.

To prevent this, the fixed time delays, of the load bus overcurrent protection TD3 and that of abnormal voltage TD1, are coordinated. TD4 is set at 150 milliseconds to allow a realistic time for secondary protection within zone 2 to operate, while TD1 is set at 250 milliseconds. This allows TD4 to operate first, removing the fault by load bus overcurrent protection, and the sub-system voltage to recover to normal after the transient condition without operating the sub-system abnormal voltage protection.

The circuits used to provide the above protection are shown in Figure IV in the blocks marked CS3, CS4, TBC-LBC OC LOGIC, Tie Bus OC TD5, DCP, LB OC TD4. The Master Royer oscillator and transductor elements T5 and T6.

3. System Protection for Feeder Faults Occurring Within Zone Three. (Reference Section II.C.1.). System faults occurring within Zone Three for any sub-system must isolate that sub-system from the system tie bus only.

A fault occurring within this zone is supplied by each sub-system through its tie bus contactor. The fault current is sensed by both the sub-system load bus and tie bus overcurrent sensing circuits. The tie bus overcurrent sensing circuit provides a signal to:

a. Lockout the operation of the load bus overcurrent protection.
b. Start fixed time delay, TD4.

If the fault condition is not cleared within 150 milliseconds, a signal is provided by TD4 to:

c. Trip the sub-systems TBC, isolating the sub-system from the tie bus.
d. Lockout any close signal to the TBC.
e. Lockout a close signal to the load division control circuit.
f. Remove the parallel system operation lockout for abnormal voltage protection.

The sub-system is then isolated from the system tie bus, and will operate as an isolated system.

For a sub-system operating as an isolated system and connected to the tie bus, the system protection described above also applies, and the same degree of protection is provided.

The circuits used to provide the above protection are shown in Figure IV in the blocks marked CS4, TBC-LBC OC LOGIC, Tie Bus OC TD5, the Master Royer oscillator and transductor element T6.

The information contained in the preceding paragraphs is summarized in the truth table of Chart I. An example on the use of the truth table is given in Appendix III of this report. The information contained within the truth table was used to provide a detailed logic block diagram to aid in designing circuits required to provide automatic protection and paralleling of static inverters. The logic block diagram is shown in Figure III of this report.

A schematic diagram of the actual circuits designed to provide the automatic protection and paralleling as indicated by the truth table, and logic block diagram was prepared and is shown in Figure IV of this report.

Converter System Automatic Protection and Paralleling Truth Table

CHART I

Symbol	Independent Variables		Conditions 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
A	Overvoltage			1		1		0	0														
B	Undervoltage				1		1	0	0														
D	Over-Undervoltage Fixed Time Delay	TD1		1	1			0	0														
E	Power Ready Fixed Time Delay	TD2		0	0	1	1	0	0														
F	Load Bus Voltage Automatic Paralleling									1													
G	Tie Bus Voltage Automatic Paralleling									1													
H	Differential Current Protection	ZONE 1										1	0	0									
I	Load Bus Overcurrent Protection	ZONE 2										Ø	1	1									
J	Load Bus Overcurrent Fixed Time Delay	TD4										0	0	1									
K	Tie Bus Overcurrent Protection	ZONE 3										Ø	1	0									
M	Tie Bus Overcurrent Fixed Time Delay	TD5										0	1	0									
N	Load Division Protection										1												
O	Load Division Protection Fixed Time Delay	TD6									1												
P	Power Ready Lockout of OV-UV Protection			0	0	1	1	0	0														
Q	Abnormal Voltage Parallel System Operation - Lock	TD2		0	0							1	1	0									
R	Manual Override Switch - Automatic Position		1	1	1	1	1	1	1	1	1	1	1	1	1								
S	Manual Override Switch - Manual Position															1	1	1	1	1	1		
U	Converter Control Switch - Close		1																				
V	Converter Control Switch - Trip														1								
W	Converter Control Relay - Manual Control Switch	CLOSE																			1		
X	Converter Control Relay - Manual Control Switch	TRIP														1							
Y	Load Bus Contactor - Manual Control Switch	CLOSE															1						
Z	Load Bus Contactor - Manual Control Switch	TRIP																1					
a	Tie Bus Contactor - Manual Control Switch	CLOSE																	1				
b	Tie Bus Contactor - Manual Control Switch	TRIP																		1			
c	Tie Bus Voltage - Dead Tie Bus								0	1													
	Dependent Variables																						
C_1	Converter Control Relay	CLOSE	1																		1		
C_2	Converter Control Relay	TRIP		1	1	1	1					1		1	1	1							
C_3	Converter Control Relay Close Signal Lockout			1	1	1	1					1		1	1	1	1						
L_1	Load Bus Contactor	CLOSE						1									1						
L_2	Load Bus Contactor	TRIP		1	1							1		1	1			1					
L_3	Load Bus Contactor Close Signal Lockout			1	1	1	1					1		1	1			1					
T_1	Tie Bus Contactor	CLOSE		1	1	1	1		1	1									1				
T_2	Tie Bus Contactor	TRIP									1		1		1					1			
T_3	Tie Bus Contactor Close Signal Lockout										1		1		1					1			
PRL	Power Ready Time Delay TD2 Lockout			1	1																		
AVL	Parallel System Operation Lockout of Abnormal Voltage									1													
LDCC	Load Division Control Circuit	CLOSE							1	1													
LDPC	Load Division Protection Circuit	CLOSE							1	1													
LDCT	Load Division Control Circuit	TRIP									1	1	1		1								
LDPT	Load Division Protection Circuit	TRIP									1	1	1		1								

Legend

0 - Indicates this condition does not exist

1 - Indicates this condition does exist

Ø - Either a 0 or 1 condition may exist (don't care).

NOTE: For an explanation on the use of this table see Appendix III of this report.

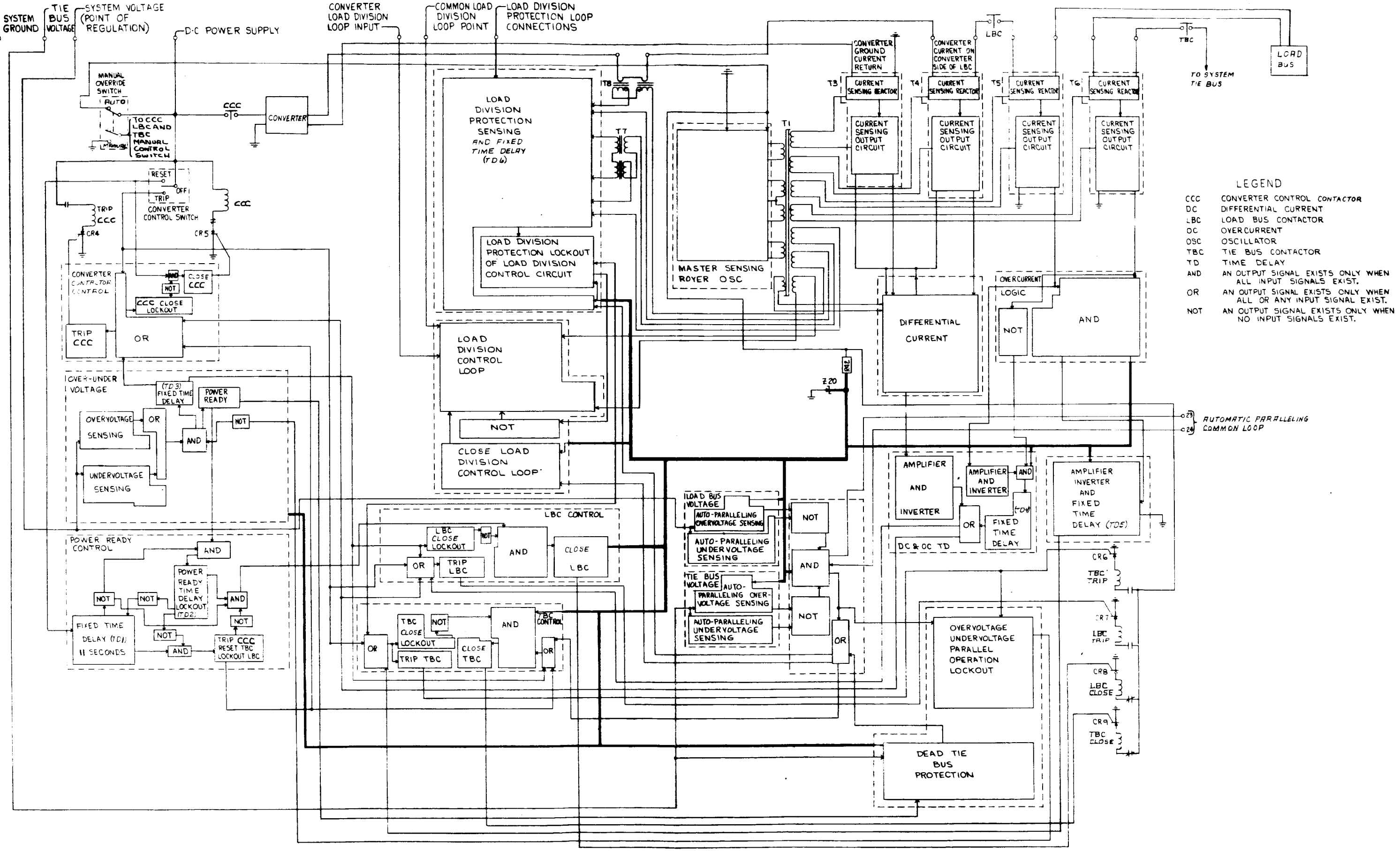

Figure III. Paralleled Converter System Automatic Protection and Paralleling Logic Block Diagram

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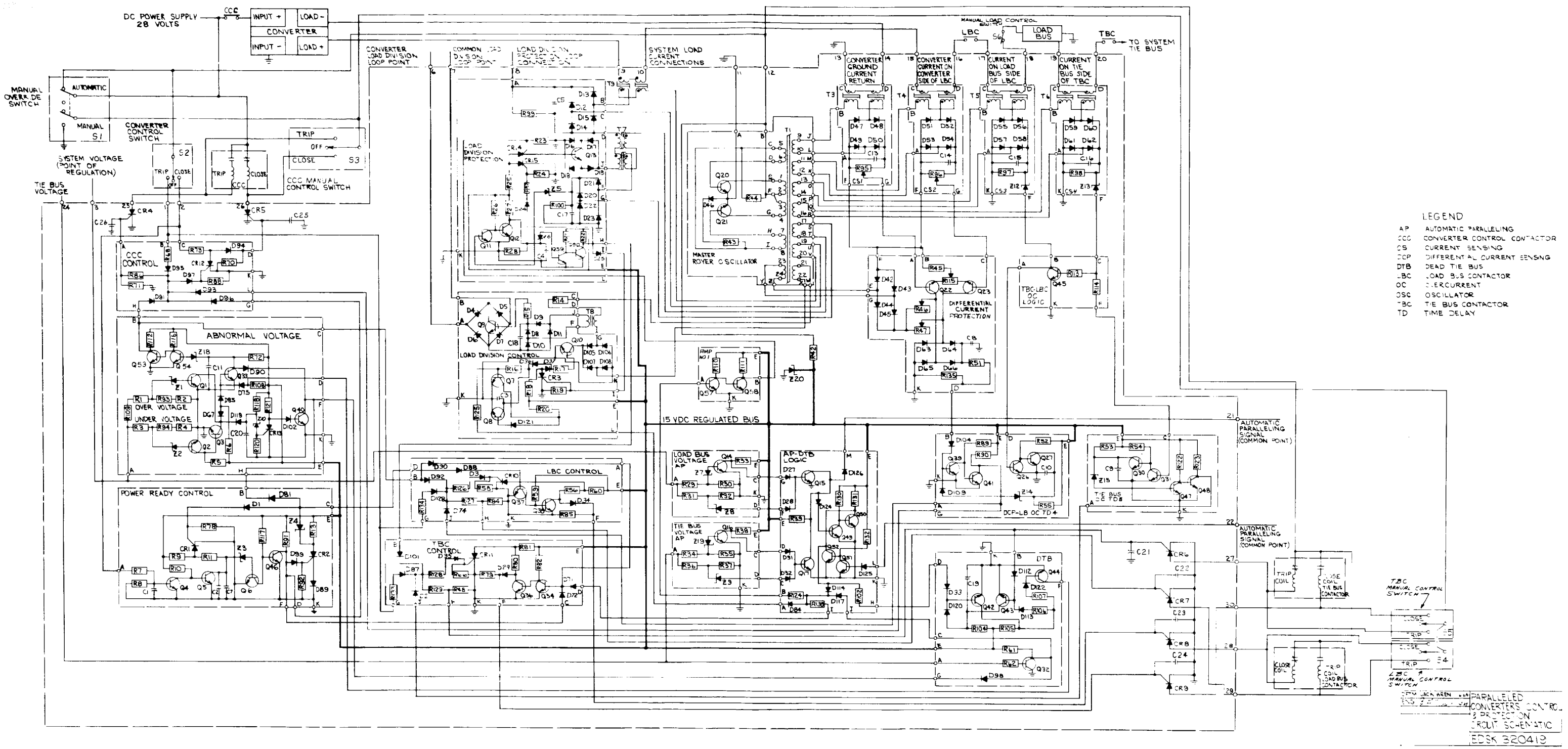

Figure I V. Paralleled Converter System Automatic Protection and Paralleling Circuits Schematic

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SECTION IV

INVERTER SYSTEM AUTOMATIC PROTECTION AND PARALLELING

A description of the automatic protection circuits for the abnormal system conditions described in Section II of this report and the automatic paralleling circuits for inverters are included in this section. These circuits are completely static and utilize no relays to provide their functions.

The contactors described in this section are used for the same reasons indicated in the introductory paragraphs of Section III. A description of the contactors is provided in Appendix II of this report.

This section of the report describes the circuits which are illustrated in the inverter schematic diagram, Figure VI . A logic block diagram for the inverter system, Figure V is also provided. The truth table, Chart II, ties in the evaluation which led to the completion of the two figures mentioned above. A brief description of this evolution will be given in Appendix III.

A. SYSTEM SWITCHES FOR AUTOMATIC OPERATION.

The discussion on system switches for converters under Part A of Section III also applies to inverter systems. The connections to these switches for inverters are illustrated in Figures V and VI of this report.

B. GENERAL.

1. Circuit Description. The circuits necessary to provide the protection shown in the logic block diagram, Figure V, are described below. The circuits needed for each function are illustrated in the schematic diagram, Figure VI. A general discussion is given first, followed by an analysis of each circuit.

2. General Circuit Discussion. Most of the protection circuits used receive an analog input from the system and transform it into a digital output. This is done by utilizing the threshhold properties of the Zener diode which will not conduct below a predetermined input voltage level and will conduct above this level. Conduction of the Zener diode results in activation of the switching portion of the protection circuit which then

produces a constant output as long as the Zener diode conducts. The outputs of the switching portions of the protection circuits are fed into locking circuits which lock onto themselves and provide a continuous positive output signal until they are reset by removing their d-c supply voltage. These locking circuits are flip-flops which utilize positive feedback to hold themselves on. The outputs of the flip-flops are used to provide the necessary action indicated by the various fault conditions.

C. INVERTER CONTROL RELAY.

Power to the inverter in each sub-system is controlled by the inverter control relay. During automatic operation, this control is provided through the ICR close and the ICR trip amplifiers shown in schematic diagram, Figure VI. The ICR close amplifier receives a signal when the inverter control switch is placed in the close position, thus, energizing the relay close coil. This closes the main relay contacts and supplies power to the inverter.

The inverter is shut down by either placing the inverter control switch in the trip position or by providing a signal from one of the inverter protection circuits. Either situation supplies a signal to the ICR trip amplifier which energizes the relay trip coil and interrupts power to the inverter. When the inverter control switch is opened, resetting the sub-system by opening and reclosing, the manual override switch is not required. However, if the inverter control relay is tripped because of a fault signal, resetting is required before power can again be applied to the inverter. This unlocks the activated protection circuit and removes its signal.

D. POWER READY.

Power ready protection is provided by combining the outputs of the over-undervoltage and over-underfrequency circuits through a common line to deliver an input to the start time delay. The start time delay, shown in Figure VI is an eleven second time delay. It is started at the time power is applied to the inverter by closing the inverter control relay and runs as long as it receives an output from the over-undervoltage or over-underfrequency circuits. An output from any of these circuits indicates a no power ready condition. If this condition exists for 11 seconds the start time delay will lock onto itself and produce a positive output. This output will trip the inverter control relay, shutting down the inverter; and will close the tie bus contactor, connecting the load to the tie bus. The start time delay circuit will continue to provide an output until is is reset by operation of the manual override switch.

If the no power ready condition is removed before the time delay runs out by disappearance of over-under voltage and over-underfrequency signals at the input of the time delay, the time delay will automatically stop timing out. At the same time, the LBC close amplifier turns on. This amplifier is held

locked out as long as a signal is fed into the start time delay. This provides a positive signal to close the load bus contactor which connects the load to the inverter.

E. LOAD BUS CONTACTOR.

Power from each inverter to its own load is controlled by the load bus contactor. Automatic operation of this contactor is provided through the LBC close and LBC trip amplifiers, shown in Figure VI. Whenever the inverter has been started and a power ready condition exists (no over-undervoltage and no over-underfrequency), a signal is supplied to the LBC close amplifier which energizes the load bus contactor close coil and connects the inverter to its load. The load bus contactor is opened by either shutting down the inverter, with the inverter control switch, or by providing a signal from one of the inverter protection circuits. In either case, the LBC trip amplifier receives a signal and energizes the contactor trip coil to trip the contactor and isolate the inverter from its load and the tie bus. As with the inverter control relay, intentionally shutting down the sub-system does not require resetting to operate the load bus contactor. However, if a fault condition caused the load bus contactor to trip, resetting is necessary. A signal to the LBC trip amplifier also disables the LBC close amplifier to prevent cycling.

F. OVER-UNDERVOLTAGE PROTECTION.

The overvoltage protection circuit designated OV, Figure VI, rectifies and filters the three phase bus voltage to provide a d-c voltage proportional to the inverter a-c output. It senses the highest phase voltage to provide this output. The potentiometer is adjusted so that the Zener diode will begin to conduct and provide an overvoltage output. When the load bus voltage exceeds 120 volts a-c rms at start up, this output indicates a no power ready condition and keeps the LBC close amplifier locked out as long as the signal is present. It also activates the 11 second start time delay circuit which shuts down the sub-system inverter and connects the load to the tie bus. This is accomplished by automatically closing the tie bus contactor if the overvoltage condition persists long enough for the time delay to run out. If the overvoltage disappears and a power ready condition is attained before the time delay runs out, the load bus contactor will connect the inverter to the load. After this time, if an overvoltage condition develops, the overvoltage circuit output will be received by the run time delay circuit which is 250 milliseconds in duration. Activation of this time delay circuit opens the inverter control relay and load bus contactor and closes the tie bus contactor. This action shuts down the inverter, isolates it from the load and connects the load to the tie bus. The load will then be supplied by other paralleled sub-systems.

The undervoltage circuit (shown as UV, Figure VI) is designed to sense the lowest phase of the inverter output voltage and utilizes a Schmitt trigger circuit to provide an output as long as the inverter output voltage remains below 105 volts a-c rms. The undervoltage circuit input network rectifies and filters the three phase load bus voltage and transmits the signal through a Zener diode to the trigger circuit. The potentiometers in this circuit provide a separate adjustment for each phase. Similar to the overvoltage circuit, an output from the undervoltage circuit indicates a no power ready condition at start up. The sequence of sub-system operation described above for an overvoltage condition applies also for an undervoltage condition.

G. OVER-UNDERFREQUENCY PROTECTION.

The over-underfrequency circuit (OF-UF, Figure VI) is a saturable reactor type frequency sensing circuit. The saturable reactor utilized in this circuit is very insensitive to sub-system a-c output voltage magnitude fluctuations but is sensitive to frequency. Therefore, it is very reliable as a frequency sensor. The output of the saturable reactor is fed through a bridge rectifier and a filter network to produce a voltage output proportional to frequency.

Two potentiometers, one for overfrequency adjustment and one for underfrequency adjustment, are provided. The overfrequency and underfrequency adjustments are set so that the circuit will produce a continuous output when the sub-system frequency is above 405 or below 390 cycles per second. Again, an output from the over-underfrequency protection circuit indicates a no power ready condition. The system operation at start up and the system operation sequence discussed above for an overvoltage condition applies for both over and underfrequency conditions as well.

H. TIE BUS CONTACTOR.

The tie bus contactor and associated circuits are utilized to control paralleling of the sub-system to the rest of the system. Automatic operation of this contactor is supplied through the TBC close and TBC trip amplifier (Figure VI). The tie bus contactor is closed by receiving a signal through its close coil from the TBC close amplifier for two conditions. First, during normal sub-system start up when conditions for paralleling are proper, the automatic paralleling circuit will provide a signal to the TBC close amplifier to parallel the sub-system. Second, particular faults (such as differential protection and no power ready) will cause the respective protection circuits to provide a signal to the TBC amplifier to close the TBC, connecting the load to the tie bus. This same fault will isolate the load from the inverter by opening the load bus contactor.

The tie bus contactor is opened by either shutting down the inverter with the inverter control switch or by providing a signal from protection circuits which indicates a fault requiring sub-system isolation. Either of these situations will provide the TBC trip amplifier with a signal to energize the tie bus contactor trip coil and isolate the sub-system from the tie bus. A signal to the TBC trip amplifier disables the TBC close amplifier to prevent cycling. Intentionally shutting down the subsystem does not require resetting to operate the tie bus contactor. Resetting is necessary only if a fault caused the initial tie bus contactor trip.

I. AUTOMATIC PARALLELING OF STATIC INVERTERS.

To satisfactorily parallel a sub-system to the tie bus a definite sequence must be followed to assure that certain requirements are fulfilled. The requirements are:

1. The oncoming inverter must be in a power ready condition - its frequency and voltage must be within prescribed limits.
2. The countdown circuits of the oncoming inverter must be in phase with the countdown circuits of the other inverters which are paralleled to the tie bus.

The phase of the output voltage of the inverter to be paralleled, relative to the system tie bus voltage, is meaningless here since it depends upon the amount of load on the inverters as described in Section II.D.5. of this report.

3. The frequency of the oncoming inverter must be locked to the system tuning fork frequency reference when its phase is correct. It must remain in phase with all other paralleled inverters after being locked in.

If no other inverters are connected to the tie bus, a dead bus condition exists. In this case, requirements 2. and 3. above may be disregarded since no problem can exist when connecting the first sub-system to the tie bus. However, to provide optimum system performance and protection it is mandatory that the first inverter being connected to the tie bus be in a power ready state and be locked to the system tuning fork frequency reference. The countdown circuit output of the first inverter will be used as a reference for all other inverters to be paralleled. The circuits required to perform these functions are shown in the schematic diagram, Figure VI.

To assure that the first requirement is met, the frequency locking and automatic paralleling circuits of the oncoming sub-system are locked out until a power ready condition exists. As soon as the proper output is attained,

the inverter is connected to its load by operation of its load bus contactor. This action unlocks and starts a time delay which is called the automatic paralleling time delay. This time delay is provided to override possible system transients caused when the inverter is connected to its load. A value of 100 milliseconds is considered sufficient for this time delay. The time delay circuit prevents the inverter from being locked onto the system frequency reference and from being paralleled until the duration of the time delay.

When the duration of the time delay has been reached, the frequency locking circuit is activated. It is then ready to receive a signal from the automatic paralleling circuit to lock the inverter to the system frequency reference. At this time, the automatic paralleling circuit of the oncoming inverter compares the paralleling pulses from its countdown circuits with the system reference paralleling pulses. The pulses are periodic and occur at the rate of 400 pulses per second (the same as system a-c output frequency).

When these two pulse trains become in phase, the automatic paralleling circuit locks onto itself and provides a continuous signal to the frequency locking circuit. The inverter is then locked in-phase with the system frequency. At the same time, the automatic paralleling circuit feeds a signal to the TBC amplifier which parallels the sub-system to the tie bus by closing the tie bus contactor.

If a dead bus condition exists, the system reference pulses will be absent. The input to the automatic paralleling circuit will then appear the same as if the system pulse train were present but coincident with the pulse train from the oncoming inverter. Since this is the proper input to the automatic paralleling circuit for system paralleling, the circuit will initiate the paralleling sequence and connect the sub-system to the tie bus; therefore, the automatic paralleling circuit will properly connect the sub-system to the tie bus regardless of whether the tie bus is dead or whether other systems are paralleled to it.

The following is a functional description of the dead bus and d-c paralleling bus circuits. This description will further clarify the way in which the system paralleling pulses are utilized to assure correct system parallel operation.

The system reference paralleling pulses are generated by dead bus and d-c paralleling bus circuits which are contained in each sub-system. These circuits are locked out until a sub-system is paralleled to the tie bus. When a sub-system is paralleled to the tie bus, a time delay holds these circuits locked out to provide time for completion of possible transients. The transients could otherwise cause the sub-system to be paralleled out of phase with the rest of the system. The system reference paralleling signal is preserved so that it can still be compared to the paralleling signal from the

oncoming inverter long enough to assure in-phase paralleling after the tie bus contactor is closed. If these circuits were allowed to operate immediately and the inverter paralleled out-of-phase, the d-c paralleling bus would indicate a frequency reference failure. Indication of a frequency reference failure would isolate all sub-systems to their own loads.

It is presently felt that this time delay must be 100 milliseconds. During the 100 milliseconds, the frequency reference failure circuit will have time to compare the system paralleling pulses to the oncoming inverter paralleling pulses. It will provide a signal to remove the inverter from the tie bus if it paralleled out of phase. If proper paralleling is accomplished, the dead bus and d-c paralleling bus circuits will be activated at the end of the time delay. These circuits are shown in the schematic, Figure VI.

J. LOAD DIVISION PROTECTION.

Load division circuits are provided within the inverters to assure equal load division between all inverters in a parallel system. However, if one of the inverter load sharing circuits should fail, that inverter may be severely damaged by abnormal system currents.

Protection against this occurrence is provided by a load division protection circuit, shown in the schematic diagram, Figure VI. Input to this circuit is provided by a current transformer loop which provides an output to the protection circuit of the faulted inverter during load unbalance conditions. At normal rated load, an unbalance of 30% will provide sufficient signal to the protection circuit to lock it on. At this point it provides a continuous signal to isolate the faulted sub-system by opening its tie bus contactor.

Since load division circuits and load division protection are necessary only during parallel operation, these circuits are locked out for each sub-system until it has been paralleled. This is accomplished by removing the associated current transformers from the system loops. In the protection circuit this is done by operation of a shorting transistor. In the inverter current transformer loop it is done by a set of tie bus contactor auxiliary contacts.

If a load division fault occurs, the load division protection circuit will isolate the faulted sub-system to its own load by tripping the appropriate tie bus contactor. The lockout of the protection circuit prevents the system from being connected back to the tie bus until the sub-system protection circuit has been reset by operation of the manual override switch.

Figure XIII of Appendix IV shows the system interconnections for the load division protection circuits.

K. INVERTER ABNORMAL CURRENT PROTECTION.

Abnormal currents may occur during either isolated or parallel system operation. During isolated operation an abnormal current condition may be the result of a differential current or a faulted load or load bus. During parallel operation abnormal current conditions may, in addition to those above, be the result of a faulted tie bus or a load division fault. The protection provided for each sub-system must be able to distinguish between the various types of faults so that selective tripping may be accomplished. The inverter protection against abnormal current conditions will be discussed in this section with the exception of inverter load division fault protection which was discussed in Section IV.J.

Abnormal current protection is provided by three circuits, the differential protection circuit (designated DP) and two overcurrent protection circuits (designated OC No. 1 and OC No. 2) in the schematic diagram, Figure VI. All these circuits receive their inputs from current transformers placed at the proper location in the system.

The current transformers which supply the differential protection circuit are connected in a loop such that they provide an output only when a difference is present between the vector sum of the currents in each phase and the total current in the ground circuit. Such a difference indicates a ground fault in either the inverter or the bus up to the load bus contactor. When a signal is received from the current transformer loop, the differential protection circuit will lock onto itself and provide a continuous output signal. This output opens the inverter control relay and the load bus contactor and closes the tie bus contactor. This removes d-c power from the inverter, isolates it from the load and tie bus, and connects the load to the system through the tie bus contactor. This circuit is designed to operate with no intentional time delay.

The current transformers which supply a signal to OC No. 1 are placed adjacent to the three phase output terminals of the inverter so that they continuously monitor the inverter output current. During isolated sub-system operation OC No. 1 is the only circuit needed to compliment the differential protection circuit and provide sub-system overload protection. It is set to provide a trip signal to open the load bus contactor if the sub-system current exceeds 120% of rated load. It contains a time delay of 160 milliseconds to provide enough time for normal system transients in the event that the inverter is suddenly loaded or unloaded. When the circuit is activated by an overcurrent condition, it locks onto itself and provides a continuous signal to the LBC trip amplifier. This opens the load bus contactor. Before normal operation can be resumed, the overcurrent circuit must be reset by operation of the manual load removal switch.

Overcurrent circuit No. 2 is similar to OC No. 1 except that it has a time delay of approximately 80 milliseconds, or one-half that of OC No. 1. The difference in time delays is to assure that the proper subsystem tripping sequence is obtained during parallel system operation. Since a signal from OC No. 2 trips the tie bus contactor and a signal from OC No. 1 trips the load bus contactor, the faulted subsystem will be isolated from the system before any inverter is isolated from its load bus.

The current transformers which supply a signal to OC No. 2 are placed between the load bus and tie bus contactors. During parallel operation these current transformers monitor the current to the load and also that from the tie bus. The double loop shown in the schematic Figure VI is provided so that the current from the tie bus (from other inverters) passes through the transformers twice while the current to the tie bus (from the same subsystem inverter) passes through them only once. Therefore, in case of a faulted load the transformers produce a signal at least twice as great as similar transformers for any other subsystems in the system. This difference in transformer outputs is used to isolate a faulted load or load bus before the overcurrent protection in any other sybsystem can take action. This is accomplished since the inverters have current limiting circuits which limit the inverter output to 150% of rated load.

If the time delay override networks in all system OC No. 2 circuits are set to provide a trip signal at 200% rated load, the subsystem having the faulted load or load bus will trip first. This is true since all other similar OC No. 2 circuits will see a maximum of 150% rated load. In this case a faulted load or load bus will cause the proper OC No. 2 circuit to trip the appropriate tie bus contactor and isolate that subsystem from the system. After the subsystem has been isolated, OC No. 1 will trip the load bus contactor and separate the inverter from its faulted load.

The previous discussion describes the operation of system protection if a load bus fault should occur. In the event of a tie bus fault, the overcurrent circuit in each subsystem will trip its tie bus contactor. This isolates all subsystems from the tie bus. Under this condition each inverter will continue to supply its own load as an isolated system.

L. FREQUENCY REFERENCE FAILURE PROTECTION

Frequency reference failure protection for parallel system operation is provided to isolate all subsystems to their own loads if the system tuning fork frequency reference fails. This protection is provided by the circuit labeled FREQ. REF. FAILURE in the schematic diagram, figure VI.

During parallel operation the frequency reference failure protection circuit continuously compares the paralleling pulses from its inverter with the system paralleling pulses to assure that they remain synchronized and in phase. If the pulses become unsynchronized the circuit locks onto itself and provides a continuous signal to open the tie bus contactor and isolate the subsystem to its own load. This fault condition causes all subsystems to become isolated since all frequency reference failure circuits will fail to see a synchronized system condition.

This circuit is also utilized to lockout a subsystem if it parallels out of phase. As described previously in Section IV. I, it compares the paralleling pulses of a subsystem which has just paralleled with the system paralleling pulses. If a phase difference is indicated, the out-of-phase subsystem is isolated by opening its tie bus contactor.

Inverter System Automatic Protection and Paralleling Truth Table
Chart II

Symbol	Independent Variables		Conditions 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A	Overvoltage			1				0	0	1																
B	Undervoltage				1			0	0		1															
C	Overfrequency					1		0	0			1														
D	Underfrequency						1	0	0				1													
E	Start Fixed Time Delay	TD1		1	1	1	1	0	0																	
F	Power Ready Fixed Time Delay	TD2								1	1	1	1													
G	Differential Current Protection													1	0	0										
H	Load Bus Overcurrent Protection													Ø	1	1										
I	Load Bus Overcurrent Fixed Time Delay													0	1	0										
J	Tie Bus Overcurrent Protection													Ø	0	1										
K	Tie Bus Overcurrent Fixed Time Delay													0	0	1										
L	Load Division Protection																1									
M	Load Division Protection Time Delay																1									
N	Automatic Paralleling and Dead Bus			0	0	0	0	1	1	Ø	Ø	Ø	Ø				1	1	1							
O	Automatic Paralleling Fixed Time Delay			0	0	0	0	0	1	Ø	Ø	Ø	Ø				1	1	1							
P	Frequency Locking								1								1	1	1							
Q	Frequency Locking Fixed Time Delay								1								1	1	1							
R	Out of Phase Paralleling																	1								
S	Frequency Reference Failure																		1							
T	Manual Override Switch - Automatic Position		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1						
U	Manual Override Switch - Manual Position																				1	1	1	1	1	1
V	Inverter Control Switch - Close		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1							
W	Inverter Control Switch - Trip																			1						
X	Inverter Control Contactor - Manual Control Switch	CLOSE																			1					
Y	Inverter Control Contactor - Manual Control Switch	TRIP																				1				
Z	Load Bus Contactor - Manual Control Switch	CLOSE																					1			
a	Load Bus Contactor - Manual Control Switch	TRIP																						1		
b	Tie Bus Contactor - Manual Control Switch	CLOSE																							1	
c	Tie Bus Contactor - Manual Control Switch	TRIP																								1
	Dependent Variables																									
I_1	Inverter Control Contactor	CLOSE	1					1	1												1					
I_2	Inverter Control Contactor	TRIP		1	1	1	1			1	1	1	1	1	1					1		1				
I_3	Inverter Control Contactor Close Signal Lockout			1	1	1	1			1	1	1	1	1	1					1						
L_1	Load Bus Contactor	CLOSE						1	1														1			
L_2	Load Bus Contactor	TRIP		1	1	1	1			1	1	1	1	1	1					1				1		
L_3	Load Bus Contactor Close Signal Lockout			1	1	1	1			1	1	1	1	1	1					1						
T_1	Tie Bus Contactor	CLOSE		1	1	1	1		1	1	1	1	1	1											1	
T_2	Tie Bus Contactor	TRIP													1	1	1	1	1	1						1
T_3	Tie Bus Contactor Close Signal Lockout															1	1	1	1	1						
PRL	Run Fixed Time Delay Lockout			1	1	1	1																			
LDCC	Load Division Control Circuit	CLOSE							1																	
LDPC	Load Division Protection Circuit	CLOSE							1																	
LDCT	Load Division Control Circuit	TRIP		1	1	1	1	1		1	1	1	1	1	1	1	1	1	1	1						
LDPT	Load Division Protection Circuit	TRIP		1	1	1	1	1		1	1	1	1	1	1	1	1	1	1	1						

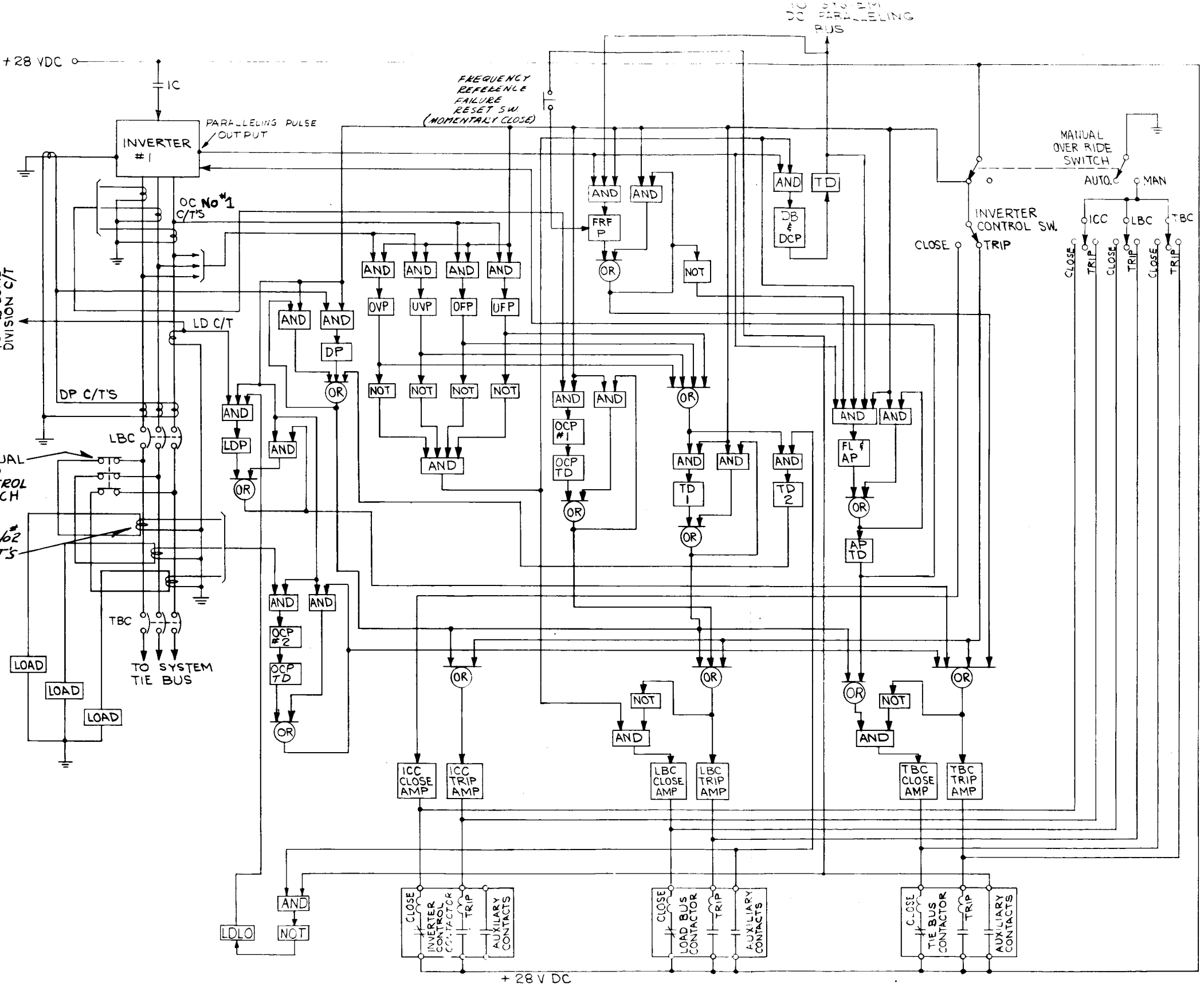
Legend

O - Indicates this condition does not exist

1 - Indicates this condition does exist

Ø - Either a O or 1 condition may exist (don't care)

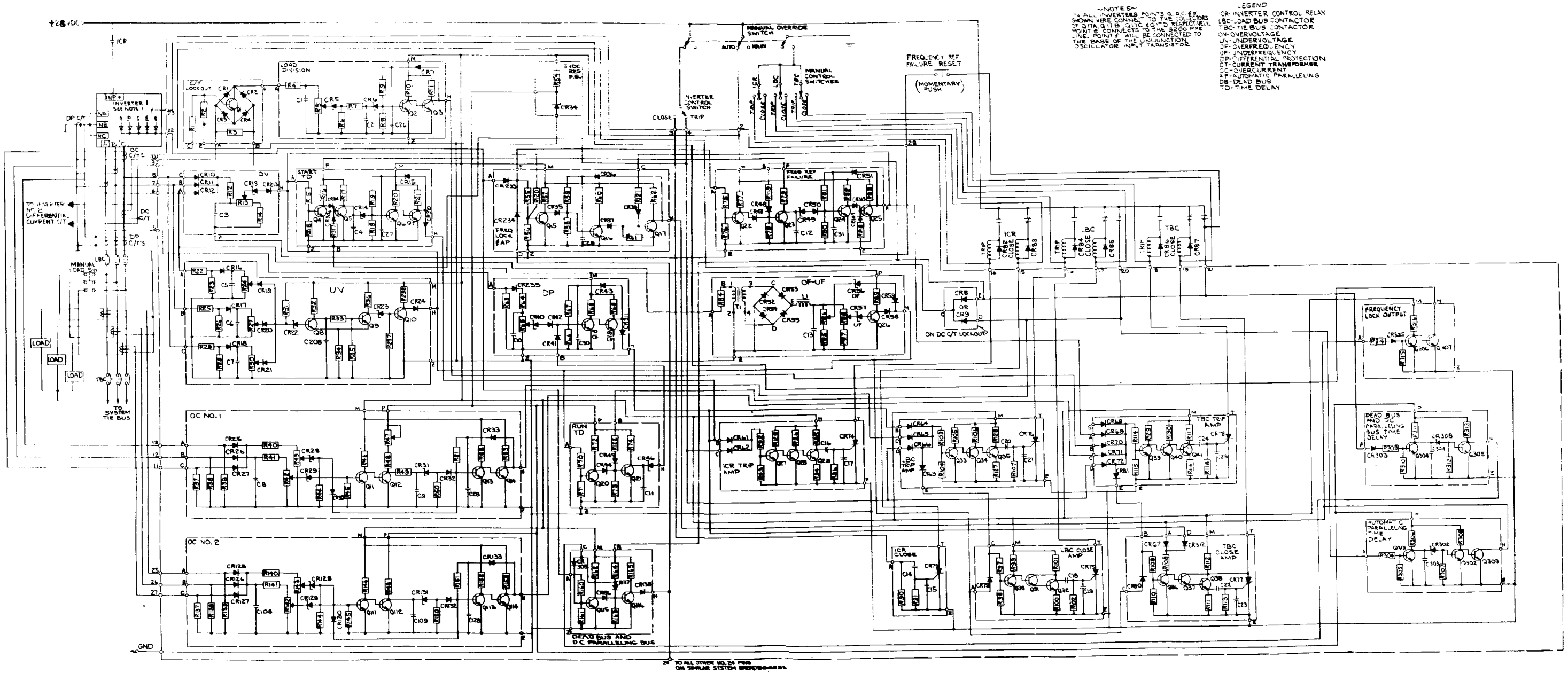
NOTE: For an explanation on the use of this table see Appendix III of this report.



LEGEND

ICC - INVERTER CONTROL CONTACTOR
LBC - LOAD BUS CONTACTOR
TBC - TIE BUS CONTACTOR
OVP - OVERVOLTAGE PROTECTION
UVP - UNDERVOLTAGE PROTECTION
OFP - OVERFREQUENCY PROTECTION
UFP - UNDERFREQUENCY PROTECTION
DP - DIFFERENTIAL PROTECTION
LDP - LOAD DIVISION PROTECTION
TD - TIME DELAY
FL - FREQUENCY LOCK
AP - AUTOMATIC PARALLELING
DB - DEAD BUS
DCP - DIRECT CURRENT PARALLELING
C/T - CURRENT TRANSFORMER
AMP - AMPLIFIER
FRFP - FREQUENCY REFERENCE FAILURE PROTECTION
LDLO - LOAD DIVISION LOCK-OUT

Figure V. Parallel Inverter System Automatic Protection and Paralleling Logic Block Diagram



NOTES:
1. ALL INVERTERS POINTS A, B, C, & N SHOWN HERE CONNECT TO THE CORRESPONDING DATA POINTS ON INVERTER I AND RESPECTIVELY. POINT B CONNECTS TO THE 3200 PPS LINE. POINTS A WILL BE CONNECTED TO THE BASE OF THE UNIJUNCTION OSCILLATOR INPUT TRANSISTOR.

LEGEND
- CR- INVERTER CONTROL RELAY
- LBC- LOAD BUS CONTACTOR
- TBC- TIE BUS CONTACTOR
- OV- OVERVOLTAGE
- UV- UNDERVOLTAGE
- OF- OVERFREQUENCY
- UF- UNDERFREQUENCY
- DP- DIFFERENTIAL PROTECTION
- CT- CURRENT TRANSFORMER
- OC- OVERCURRENT
- AP- AUTOMATIC PARALLELING
- DB- DEAD BUS
- TD- TIME DELAY

Figure VI. Parallel Inverter System Automatic Protection and Paralleling Circuits Schematic

SECTION V

CONCLUSIONS

A. A study to define the requirements for automatic protection and paralleling of static converters and inverters has been completed. The results are contained in this report.

B. Circuits meeting these requirements have been designed and will be built to demonstrate their performance. Tests will be conducted during the remaining portion of this contract.

SECTION V I

RECOMMENDATIONS FOR FUTURE WORK

To improve automatic system operation and increase its capabilities, it is recommended that the following be considered for future work.

A. The design, development, construction and testing of static load contactors for both DC and AC type loads, that are compatible with both input and output power requirements of the static converter/inverter utilized under the first portion of this contract.

B. The design, development, construction and testing of static circuits that operate in conjunction with protection and control circuits to indicate the type of system failures that occur. The information provided by these circuits will facilitate correct manual system operation.

C. The design, development, construction and testing of an automatic static load controller and programmer that is compatible with static converters or inverters. The load controller and programmer would automatically provide maximum overall system efficiency by energizing only the number of converters or inverters needed to supply the load required.

SECTION VII

APPENDIX I

APPENDIX II

APPENDIX III

APPENDIX IV

APPENDIX I

A. TRANSIENT CHARACTERISTICS OF STATIC CONVERTERS AND INVERTERS.

For either isolated or parallel system operation of static converters or inverters, transient conditions occur during which the basic system parameters of voltage, current, and (for AC systems only) frequency exceed their nominal limits. These conditions are caused by the sudden application or removal of large system loads or removal of fault conditions. The transient conditions exist for only short periods of time and are an inherent characteristic of static converters/inverters and their voltage regulating and load division control circuits. No damage to utilization equipment or the converters/inverters themselves will occur for these conditions and no system protection against them is required.

However other transient or abnormal conditions of the basic system parameters may occur which are a result of a failure in the basic control circuits. For these conditions automatic system protection must be provided which is capable of distinguishing between a normal system transient condition and an abnormal system condition. This is accomplished by using time delays, in conjunction with the system protection, sufficient to allow transient conditions to occur and steady-state conditions to be reached prior to operation of the protective circuits. The normal transient characteristics of the converter/inverter must be defined in order to determine the length of time delays required.

During the first portion of this contract, system tests were conducted where both static converters and inverters were paralleled under various conditions of initial system load and voltage. From the results of these tests the transient response characteristics of the converters and inverters were obtained and the time delays necessary in the control and protection circuits were determined. The results of the above tests are summarized below.

1. Static Converter Transient Response Characteristics.

   Three types of tests were conducted on the static converters. Each is discussed below.

   a. The first type of test consisted of paralleling two converters with identical initial loads and output voltages. The tests were run for initial system loads of 0, 25, 50, 75, 100, and 125% of rated load. Data for these tests are shown in figures 46 through 51 on pages 63 to 69 of the Third Quarterly Report. [3]

      Review of these data shows that only very slight transients occurred for any of the above test conditions. Voltage changes

were less than 5 volts from the initial voltage setting. The time duration was less than 14 milliseconds.

Since the transients caused by the above condition were so slight compared to those of paragraph b. below, they were not considered in determining the maximum transient response of the static converters.

b. The second type of test consisted of paralleling two converters with large differences in initial load or applying a large load to parallel converters.

The transients caused by these tests were the most severe obtained. The transients caused are shown in Figures VII and VIII of this appendix.

Figure VII is the oscillograph recording of the system voltage and current transient caused by placing rated load on two, paralleled, unloaded converters. This produced the most severe transient condition of all the tests conducted. The maximum time required for recovery of the system voltage was 56 milliseconds. A considerable droop of system voltage occurred, reaching a minimum of 96 volts from an initial setting of 153 volts.

c. The third type of test was to parallel two fully loaded converters with different initial no-load voltage settings. The results of these tests are shown in figures 56 and 58 on pages 74 and 76 of the Third Quarterly Report[3]. The transient conditions that resulted were negligible compared to those obtained from the tests of b. above and were not considered in determining the maximum system transient response time. Information contained in Figure VIII was taken as the maximum time duration of the transients since the transient response characteristic of the static converters is affected most severely by heavy loads.

An additional 14 milliseconds was arbitrarily added to the response time to allow for variations that may occur within the converters and during system operation which may affect the transient response. The maximum response time of the converter is then taken as 70 milliseconds. This value is considered to be the minimum time delay to be provided for protection circuits that sense abnormal system parameters during transient conditions. The protection circuits will not operate during this time period.

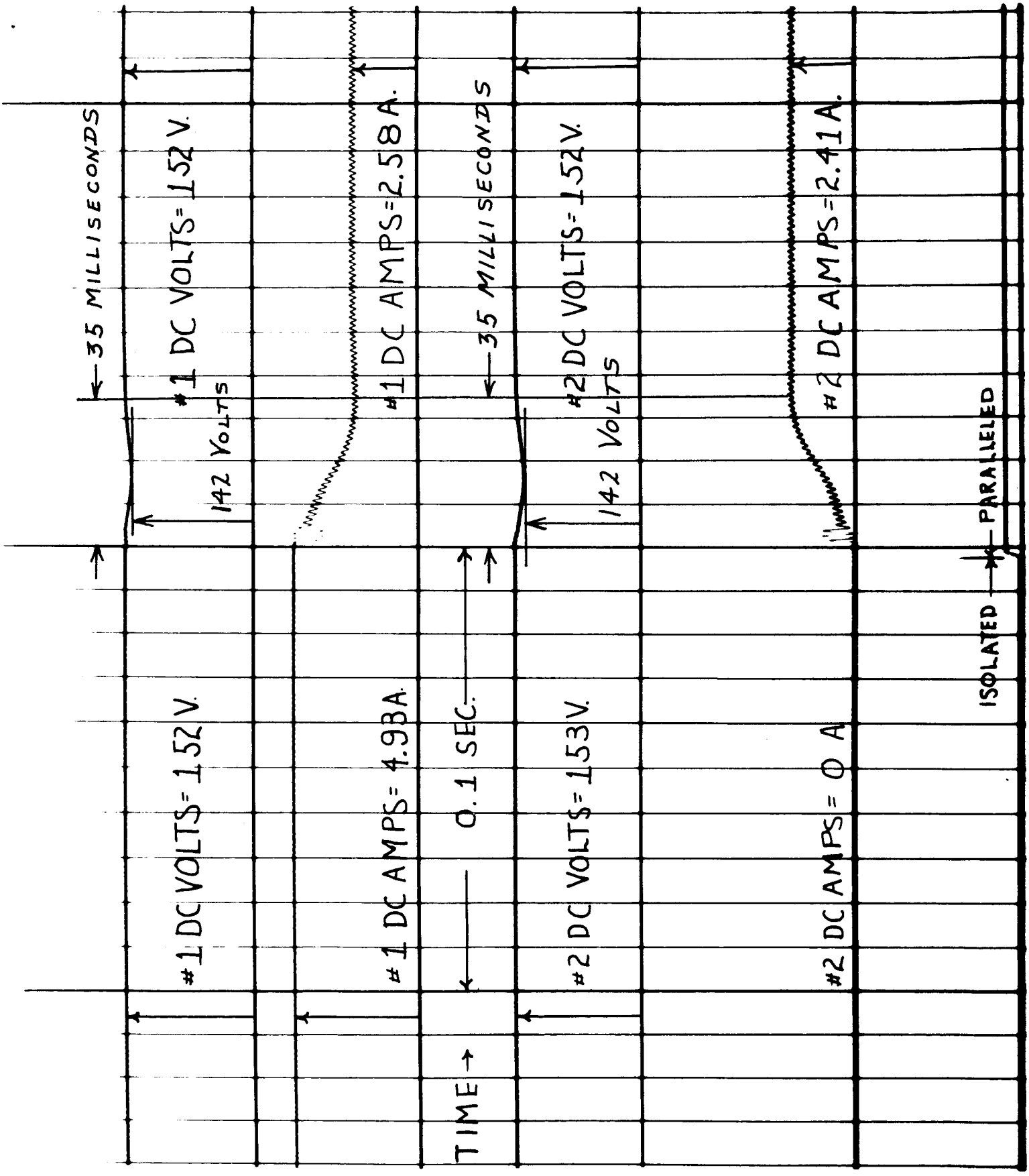


Figure VII. Oscillograph Recording of the Transient Caused by Paralleling a Loaded Converter with an Unloaded Converter

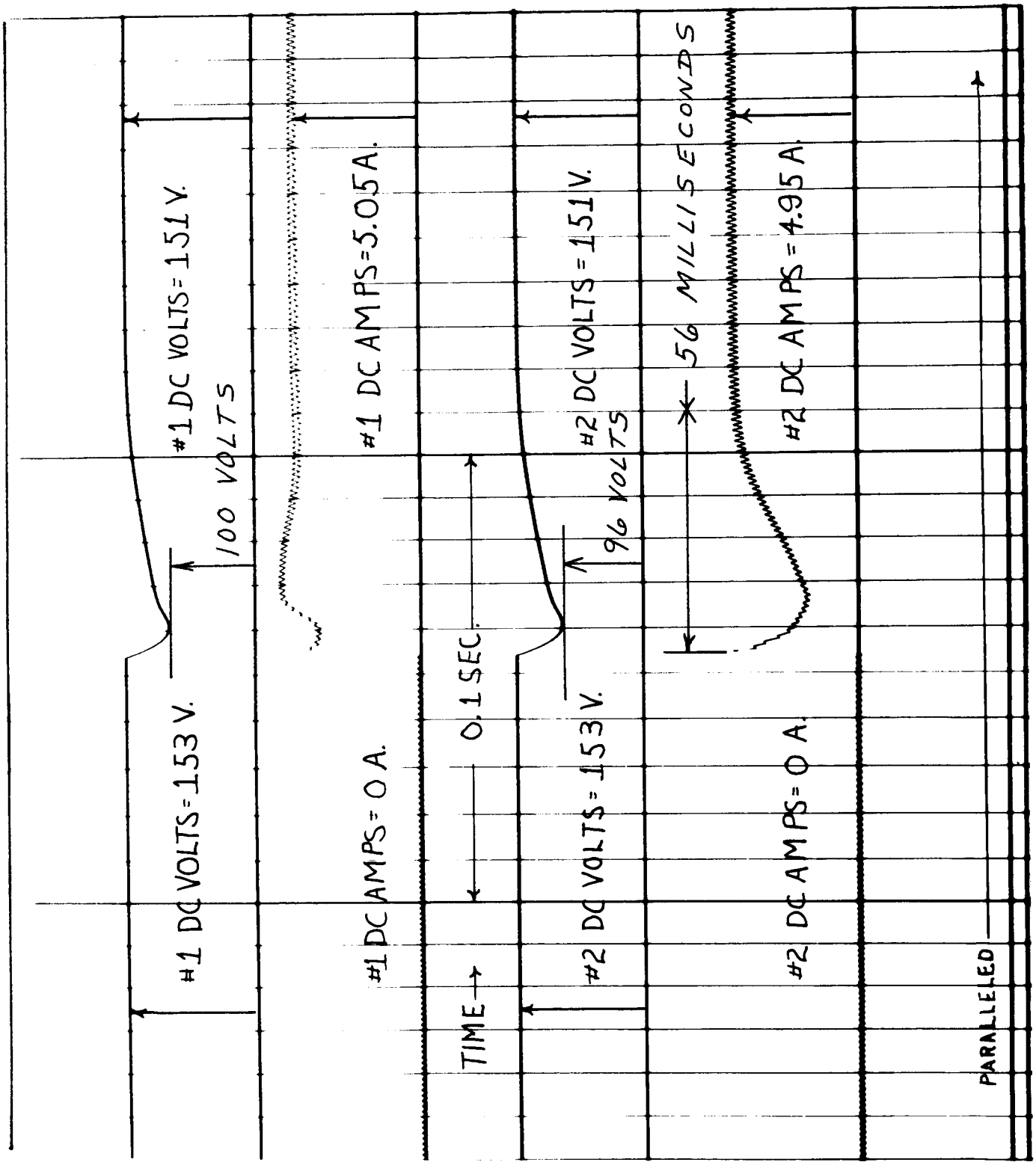


Figure VIII. Oscillograph Recording of the Transient Caused by Placing Rated Load on Two Paralleled-Unloaded Converters

2. Static Inverter Transient Response Characteristics.

Four sets of tests were conducted on the static inverters. Each is briefly discussed below.

a. The first sequence of tests consisted of paralleling two inverters, each at 100% of rated load with the power factors of 1.0, .75 lagging, .9 lagging and .9 leading. Oscillograph recordings of these tests are shown in figures 18 through 21 on pages 27 through 30 of the third quarterly report.[3] The transients produced during these tests were negligible and were not considered in determining the transient response of the static inverter.

b. The second sequence of tests consisted of paralleling inverters with unbalanced loads and suddenly applying loads to paralleled inverters. Oscillograph recordings of these tests are included in the third quarterly report on pages 32 through 39. The maximum current transient produced under these conditions was 50 milliseconds. This transient occurred when an inverter carrying rated load was paralleled to an unloaded inverter. Approximately the same transient was observed when rated load was suddenly applied to two paralleled inverters. In the second case the inverter output voltage dropped from 115 to 114.5 volts. Figure IX is an oscillograph recording taken from the third quarterly report which illustrates the second case.

c. The third sequence of tests consisted of paralleling inverters with unequal input voltages, unloaded; and paralleling them with unequal output voltages, loaded with rated current for one inverter (at power factors of 1.0 and .75 lagging). The maximum transient occurred at a power factor of 1.0. This transient was 40 milliseconds long. The results of these tests are shown on pages 42, 43, and 44 in the third quarterly report.

d. The fourth sequence of tests consisted of starting a one-eighth horsepower motor with one inverter and then with two in parallel. Figure X is the oscillograph recording from the third quarterly report which shows the transient caused when one inverter starts a one-eighth horse power motor. The output voltage in this test dropped initially to 75% of its original value. The transient caused was 140 milliseconds long.

Although the fourth test produced the most severe transients, a shorter time delay was used since the loads to be used for demonstration purposes in this program will be constant. Except for the motor test the most severe transient was 50 milliseconds in duration. Therefore, to assure that system transients have time to decay, a minimum of 80 milliseconds was chosen for all time delays in the inverter system except for protection circuits where no time delay was provided.

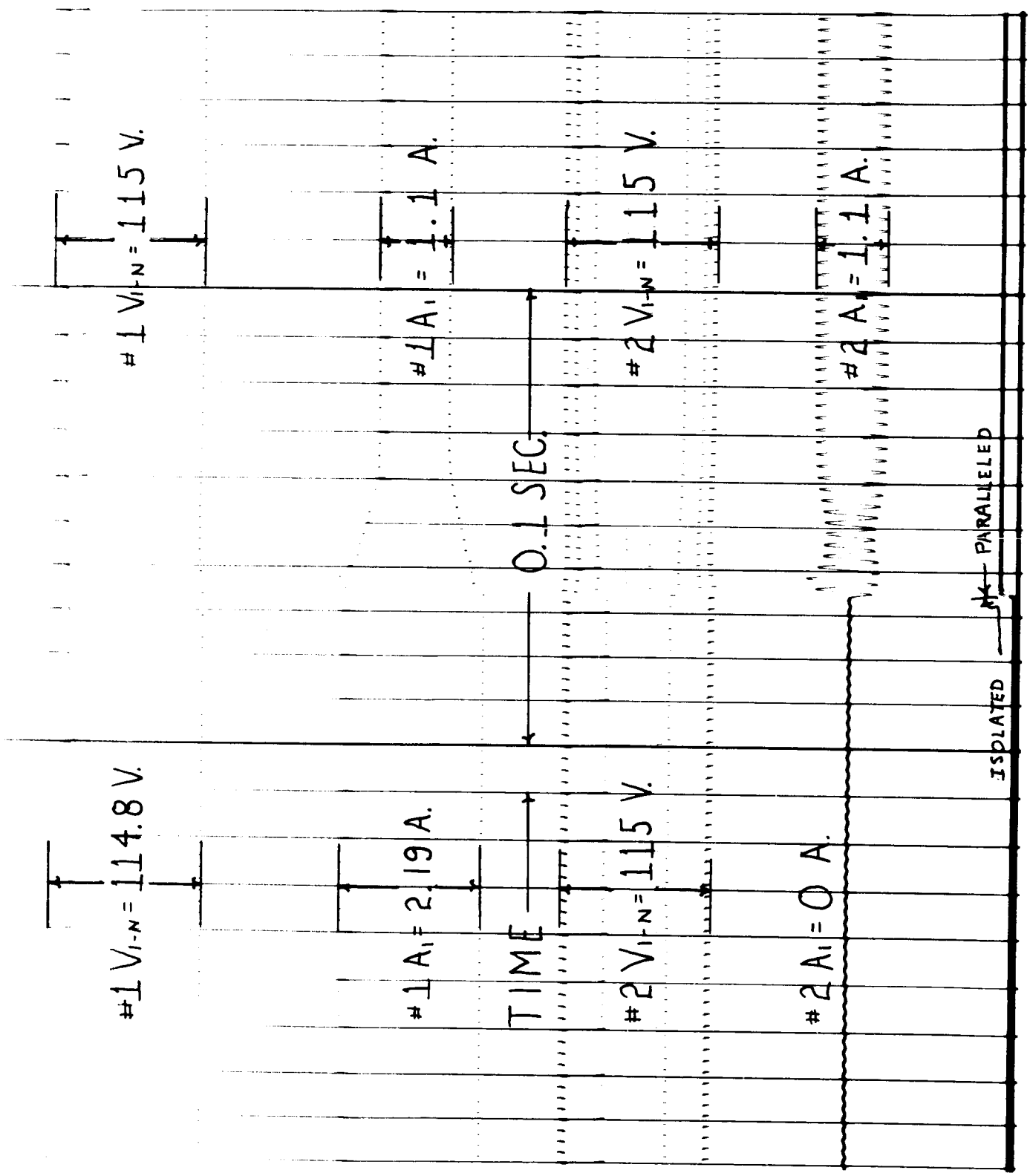


Figure IX. Oscillograph Recording of the Transient Caused by Paralleling a Loaded Inverter with an Unloaded Inverter

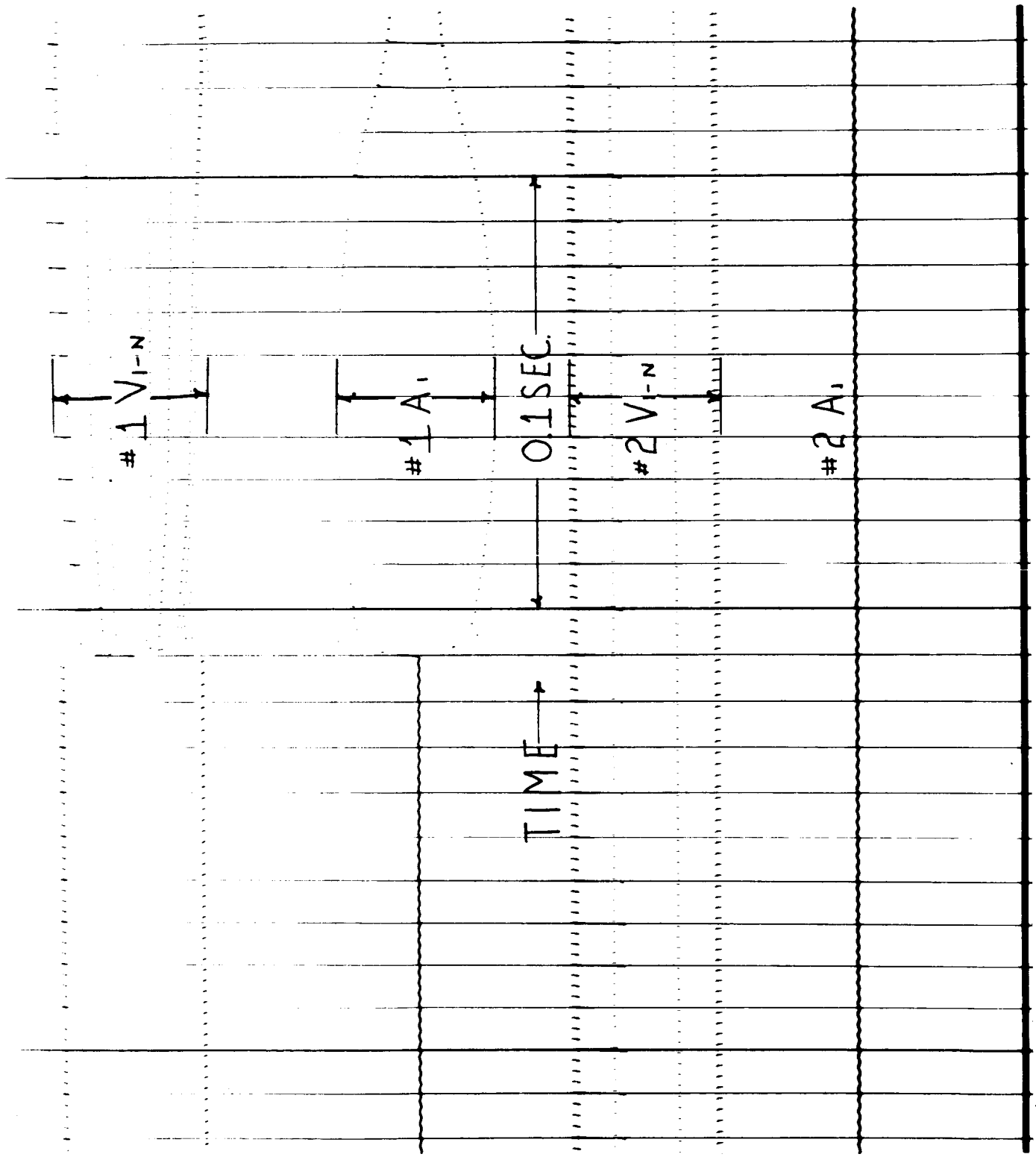


Figure X Oscillograph Recording of One Inverter Starting a 1/8 H. P. Motor

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APPENDIX II

OPERATION OF A LATCH TYPE RELAY (CONTACTOR)

Latch type relays are used to connect each sub-system converter/inverter to its power source, connect the converter/inverter to the load bus and connect the sub-system to the tie bus. Separate relays are used for each of these functions.

The relays consist of two coils (one close coil and one trip coil), a set of interconnected contacts used to interrupt the coil currents after they have been energized, and three sets of load carrying contacts. All the relay contacts are connected to a common armature which opens or closes the contacts when the relay coils are operated. A mechanical means is also provided to maintain the armature in position after the coils have been energized. A schematic diagram of the relay is shown in Figure XI. A description of its operation is given by the following example.

Assume that the close coil of the relay was the last coil operated. All the relay contacts are then as shown in Figure XI . In this position the load carrying contacts are closed and power can pass through the relay. The coil contacts for the trip coil are closed and the relay can be tripped when a ground is provided for the trip coil. When the ground is provided, the trip coil of the relay is energized and moves the relay armature in a direction to open all the load contacts, open the trip coil interrupting contacts, and close the close coil interrupting contacts. The relay will be retained in this position, by a spring, until the close coil of the relay is energized. The close coil of the relay will be energized when a ground is provided to the close coil. When the ground is provided, the close coil is energized, and the spring force is overcome. The relay armature is moved in a direction to close all the load contacts, close the trip coil interrupting contacts and open the close coil interrupting contacts. The relay is held in this position by another spring force until the trip coil is again energized, the spring force is overcome, and the relay armature is moved to the trip position.

The ground circuits for both the trip and close coils of the relay are provided by controlled rectifiers which are normally off and do not pass current until they are provided a gate signal to turn them on. This gate signal is provided

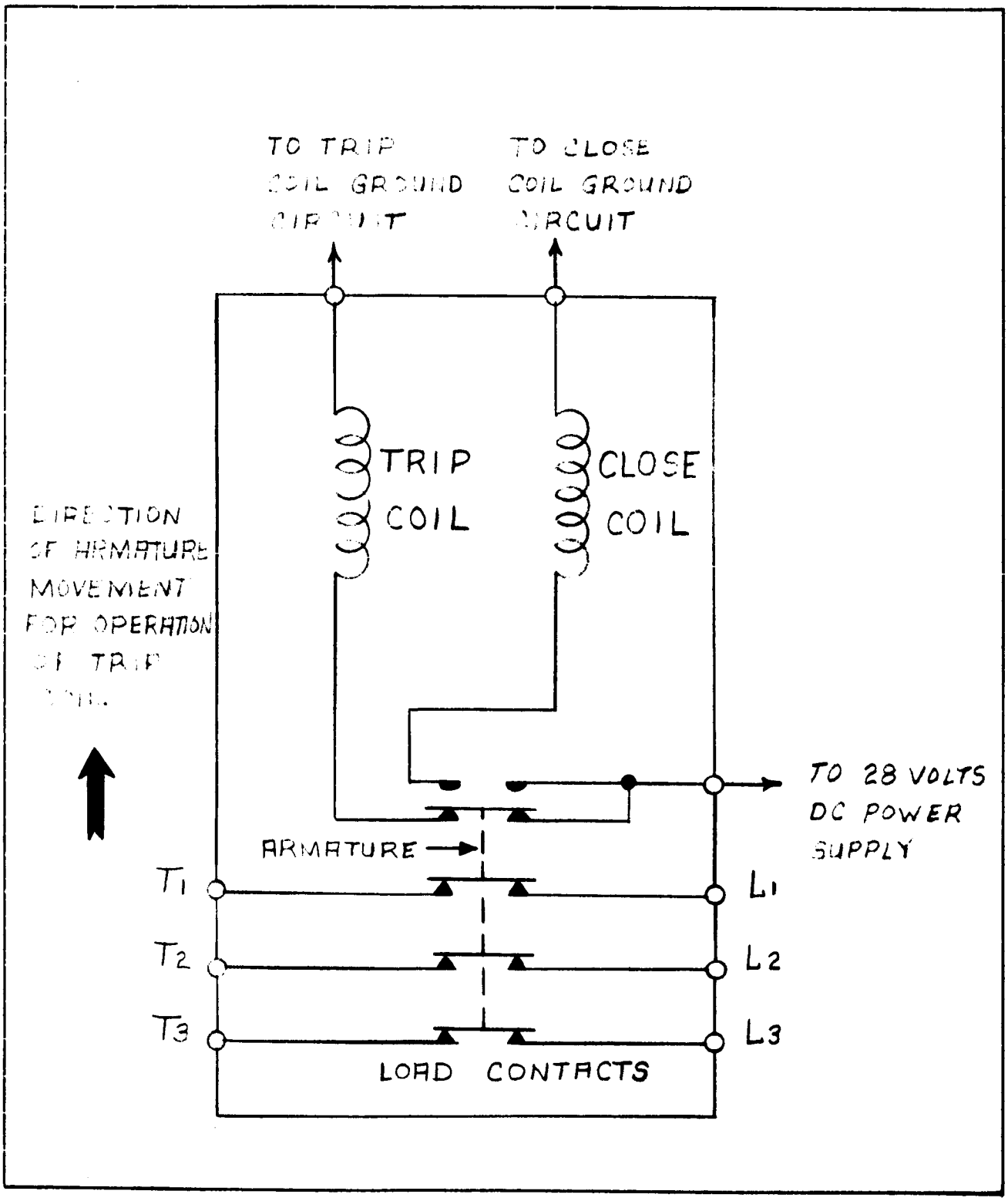

Figure XI. Latch Type Relay (Contactor)

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by the automatic protection and paralleling circuits when system conditions are such that a particular relay is to be either closed or tripped. After the controlled rectifier is turned on, it will remain on regardless of whether or not a gate signal is applied until the current through it goes to zero. This occurs when the coil interrupting contacts open after the coil has been energized, as described above.

The relays (contactors) used as part of this program are rated as follows:

A. COIL RATING

1. 28 volts d-c; operate 15 to 30 volts.
2. Close coil resistance 2.0 ohms at 25°C
3. Trip coil resistance 3.5 ohms at 25°C

B. MAIN LOAD CONTACTS RATING

1. 120 amperes at 115 volts, 400 cps, continuous.
2. 420 amperes at 115 volts, 400 cps. Carry for and interrupt after 5 seconds.
3. 4000 amperes maximum interrupting capability in accordance with MIL-C-8379A.

C. OPERATING TIME OF LOAD CONTACTS.

1. Close - 50 milliseconds maximum with 15 volts applied to close coil.
2. Trip - 15 milliseconds maximum with 15 volts applied to trip coil.

D. This relay is qualified to MIL-C-8379A.

APPENDIX III

EXAMPLE FOR USE OF THE TRUTH TABLE.

The following is an example illustrating use of the truth table given in Chart I of Section III.

The truth table summarizes the operations of the automatic protection and paralleling circuits described in Section III.

1. Explanation of Truth Table

   The truth table classifies all types of variables as either independent or dependent.

   An independent variable is one which senses system or other logic conditions and provides an output signal that indicates a given condition exists. It, acting alone or in conjunction with others, results in the operation of a dependent variable. Examples of this type of variable are the overvoltage and undervoltage sensing circuits.

   A dependent variable is a variable that has no independent output. Its operation is dictated by the information that it receives from one or more independent variables.

   There are two possible states that any variable may have. It may have an output or it may not have an output. The symbols "1" and "0" are used to identify these two conditions respectively. In some instances either condition may exist without any effect on system protection. These conditions are designated as $\emptyset$ and are "don't care" conditions.

   Contained within the truth table are the conditions that must be satisfied to provide the desired system automatic protection and paralleling. Many other combinations of conditions are possible that are not shown in the truth table, but they will not result in the desired system protection and paralleling. This excludes faults or failures of the protection circuits themselves.

2. Use of the Chart

   The dependent variables control the system through information dictated to them by the independent variables, and are the end functions for system protection or automatic paralleling. The following example is used to illustrate the use of the truth table.

Assume that it is desirable to know when the subsystem load bus contactor is tripped. This information can be obtained directly from the truth table as follows:

Find Load Bus Contactor Trip under the Dependent Variable Heading. (Symbol L_2). Read horizontally to the right. Every symbol "1" found under the columns identified as Conditions indicates that a trip signal is applied to the load bus contactor, causing the load bus contactor to trip and isolate the subsystems converter from the load bus.

The symbol "1" occurs for conditions 2, 3, 10, 12, 13 and 16.

Reading each of these columns vertically will give the conditions that must exist for the load bus contactor to trip.

Under condition 2 the symbols 1 1 0 0 0 1 exist. Reading horizontally to the left these symbols refer to the independent variables identified by the symbols A D E' P' Q' R (Unprimed symbols correspond to 1 and primed symbols correspond to 0, with 1 and 0 having the meaning previously stated.)

The specific independent variables in this example are:

A -- Overvoltage condition exists
D -- Overvoltage-Undervoltage time delay exceeded
E'-- No power ready fixed time delay exists
P'-- No power ready lockout of the OV-UV protection exists
Q'-- No lockout signal for abnormal voltage-parallel system operation
R -- The manual override switch is in the automatic position

When this combination of conditions exists, the load bus contactor receives a trip signal isolating the converter from the load bus. This same procedure can be followed for conditions 3, 10, 12, 13, and 16.

An equation using symbols can now be written for all the conditions that result in providing a signal to trip the load bus contactor. This equation is given below.

$$L_2 = ADE'P'Q'R + BDE'P'Q'R + HJ'M'QR + H'IJK'M'Q'R + SZ$$

The + symbol indicates an "or" condition which means any one of the combination of conditions will result in providing a trip signal to the load bus contactor.

The next step is to combine terms where possible, which results in the following equation.

$$L_2 = (A + B)\ DE'P'Q'R + HJ'M'QR + H'IJK'M'Q'R + RV + SZ$$

This simplification gains nothing.

3. The above procedure can be used to obtain equations for each dependent variable shown in the truth table. These equations can then be simplified to minimize the circuits and components required to provide the necessary system automatic protection and paralleling. However, as shown above for a typical example, the actual simplification obtained is negligible and does not justify utilizing this approach for circuit minimization. A simpler and more direct approach is to use the information contained in the truth table as a guide in preparation of a logic block diagram and circuit schematic for the required protection and automatic paralleling.

4. The procedure used to demonstrate the use of the converter system truth table of section III can also be applied to the truth table of section IV. Therefore the procedure is not repeated for the inverter system.

APPENDIX I V

SYSTEM INTERCONNECTIONS FOR LOAD DIVISION PROTECTION CIRCUITS

This appendix contains figures that show the necessary system interconnections for the load division protection circuits. Figure XII applies to converter systems and Figure XIII applies to inverter systems.

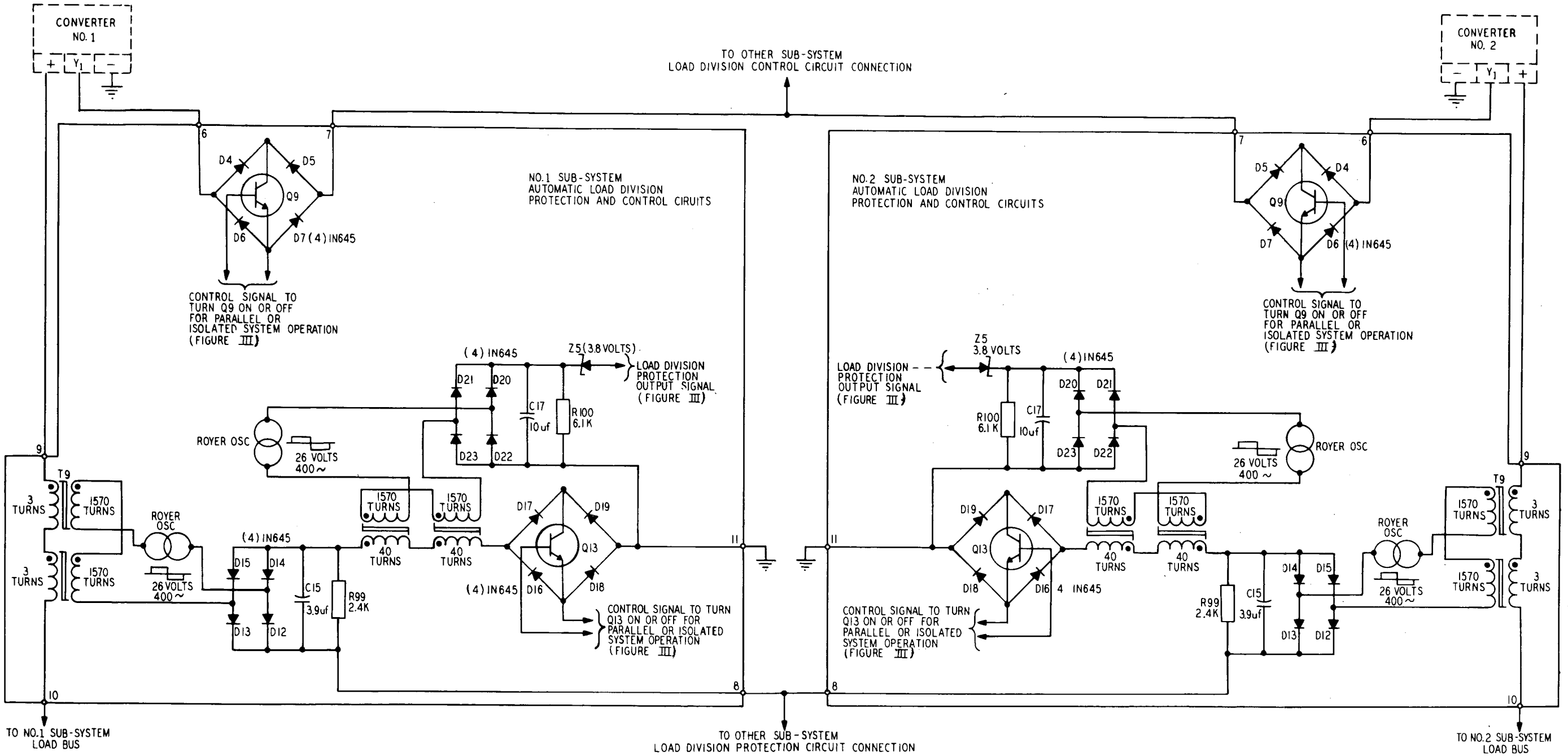

Figure XII. System Interconnections for the Load Division Protection Circuits in a Paralleled Converter System

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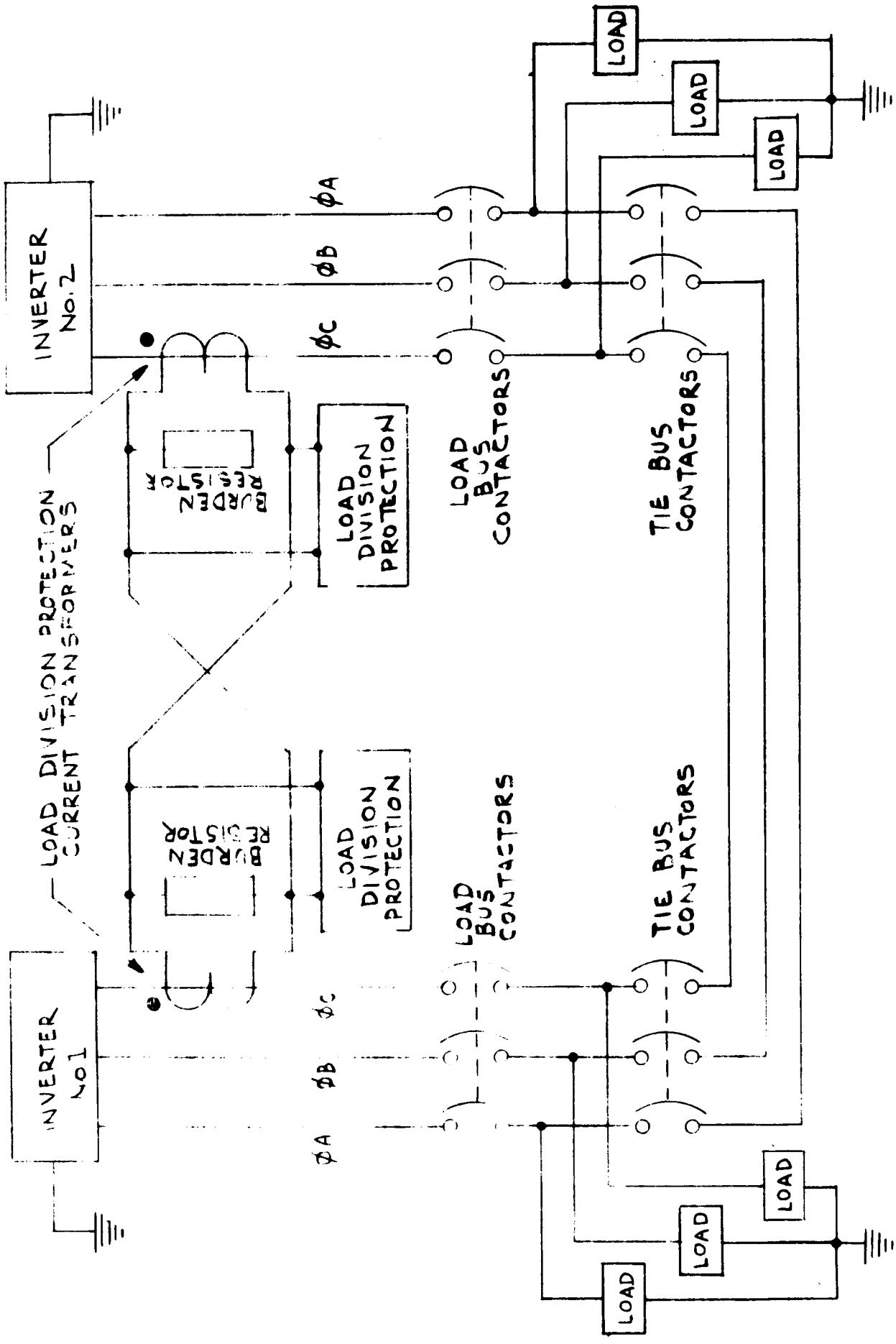

Figure XIII. System Interconnections for the Load Division Protection Circuits in a Paralleled Inverter System

SECTION VIII

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2. NASA Contract NAS 3-2792. Second Quarterly Report for the period September 28, 1963 to December 27, 1963; Parallel Inverter and Converter Operation and Improvements in Transformers.

3. NASA Contract NAS 3-2792. Third Quarterly Report for the period December 28, 1963 to March 27, 1964; Parallel Inverter and Converter Operation and Improvements in Transformers.

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